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A CAHNERS PUBLICATION

April 29, 1993

Special Report:
Mix ASIC models to win the simulation game pg 74

EDN

April 29, 1993 VOLUME 38, NUMBER 9

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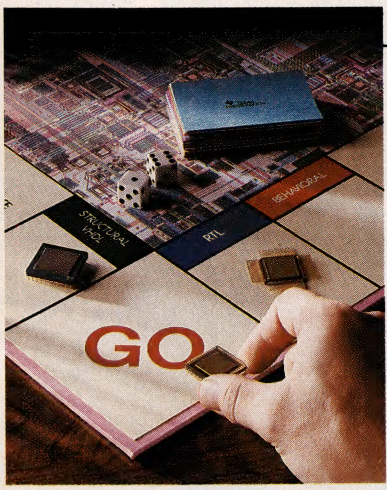

On the cover: Playing the multilevel ASIC modeling game requires finesse. Once you start off, you'll encounter ASICs with more than 20,000 gates, vendors with simulation secrets, and some closely held intellectual property. Instead of rolling the dice, read the Special Report for ways to make multilevel modeling easier. (Photo courtesy Texas Instruments Inc; art direction, Ken Martin; photography, Cece Cox) . . . . PAGE 74

Foldout Contents

Turn to the last information-retrieval service card in the back of this magazine and you'll find a foldout table of contents. Now, instead of flipping back and forth from this table of contents to the articles you want to read, you can have the convenient foldout open at all times while you're reading EDN. Use the foldout contents to mark off articles you'd like your colleagues to read or to remind yourself to copy stories for your files.

SPECIAL REPORT

DESIGN FEATURES

TECHNOLOGY UPDATE

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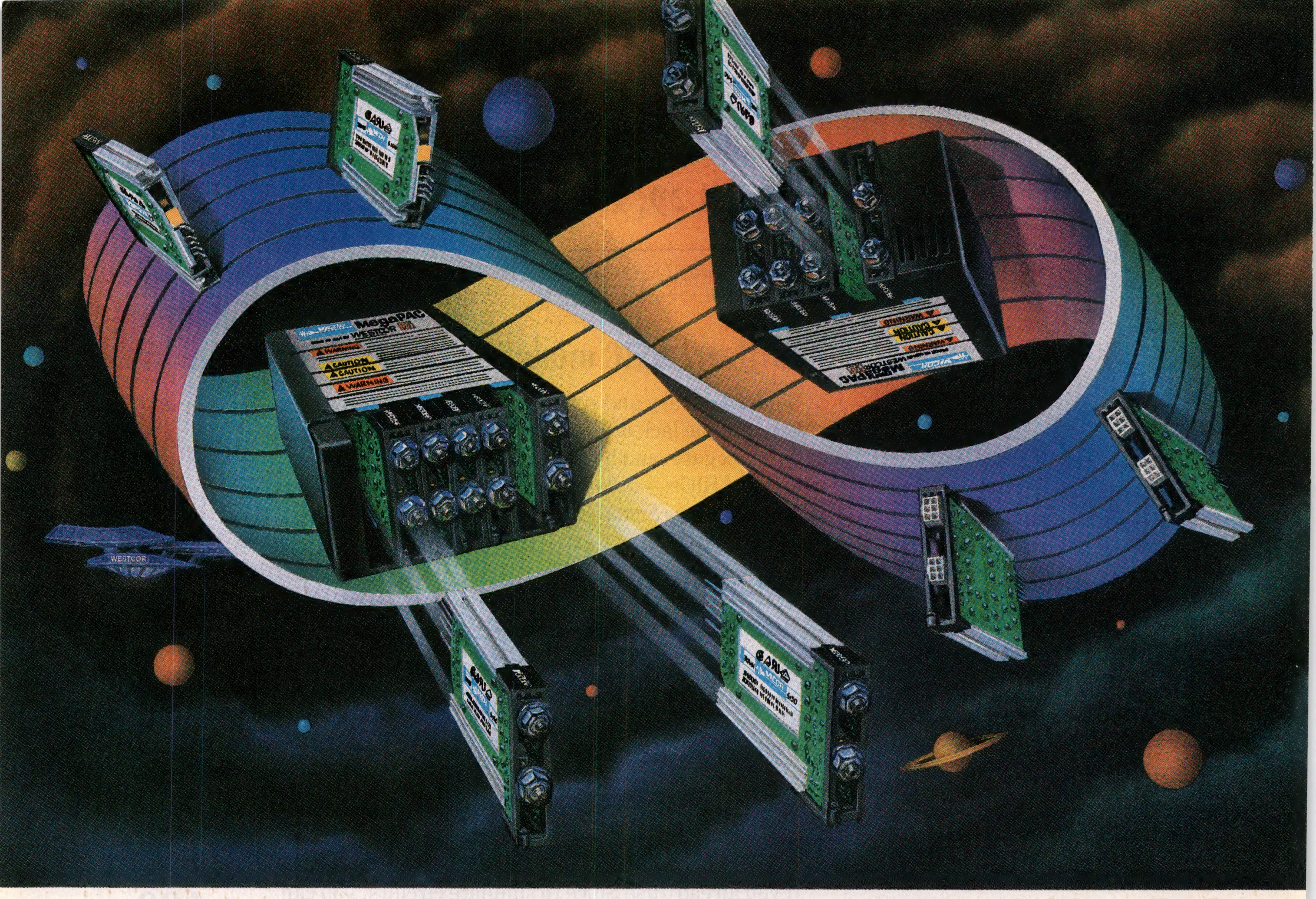

Endless Power Options

Field-Configurable MegaPAC™ Switching Power Supplies

Your opportunities are endless to mix and match MegaPAC options. And with so many possible power solutions available, you can define one precisely to fit *your* needs.

But MegaPAC flexibility doesn't end there. If your needs change, so can your switcher …which gives you another reason to choose MegaPAC power supplies: they're *the only field-configurable power supplies* on the market. To alter voltage or power levels on site, just loosen a screw, slide out a ModuPAC converter assembly, and slide in a new one. It's that simple.

Take a look at our new additions to the MegaPAC family, highlighted at right.

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NEW! Automatically senses line voltage and straps power supply accordingly.

- 85-264 VAC universal input with power factor correction ***NEW! Meets IEC 555.***

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- Up to 1600 watts total
- Up to 100 or up to 200 watts per output
- 1-16 outputs, isolated & fully regulated
- 1 to 95 VDC

ModuPAC slide-in converter assemblies:

- Standard—one output, up to 200 watts
- ***NEW* DualPAC**™ —two outputs, up to 100 watts each
- ***NEW* TachoPAC**™ —for fast transient response to high-speed load changes
- ***NEW* RamPAC**™ —for very low noise
- ***NEW* VXI Option**—for low noise and low ripple to meet instrumentation standard VXI

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EDN

April 29, 1993

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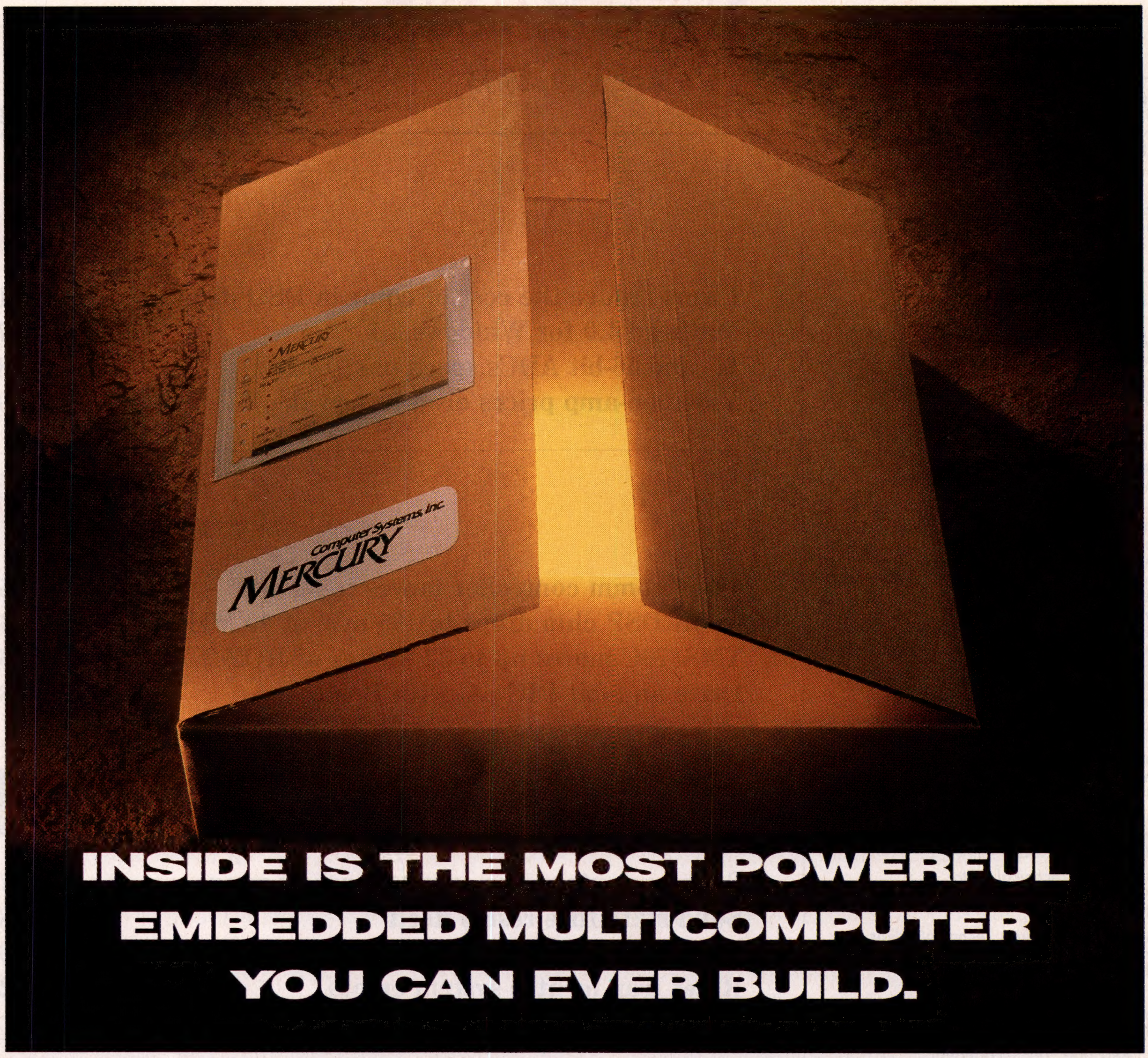
PRODUCT UPDATES

PROCESSOR UPDATES

DESIGN IDEAS

NEW PRODUCTS

DEPARTMENTS



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CIRCLE NO. 112

A summary and analysis of articles in this issue

Sooner or later, improvements and advances in technology are going to affect you and your products. The articles in this issue of EDN concentrate on some of those developments that may not affect you today, but that you may soon need to consider. Many of those developments are the same story: Some things get bigger so that everything else can get smaller and cheaper. Of course, that doesn't always make your life easier right away.

In the Special Report on **Multilevel ASIC modeling**, John Napier and Julie Anne Schofield explore the problems you'll encounter if you decide to put a µP on your ASIC. Gate counts on ASICs are growing rapidly. Although you may not use an ASIC with more than 20,000 gates today, chances are you will by the end of the year. So, now that there is room to stick a µP on an ASIC, you have to figure out how to model the ASIC to make sure it works.

Sounds simple, but as John reveals on this issue, "capitalism collides with engineering." Semiconductor vendors won't give you detailed simulation models of their chips because they don't want you to reverse engineer them. But they will give you higher-level models. That leaves you with the problem of how to perform multilevel modeling. John explores some of the techniques that make multilevel modeling easier as well as tackling the issue of intellectual property.

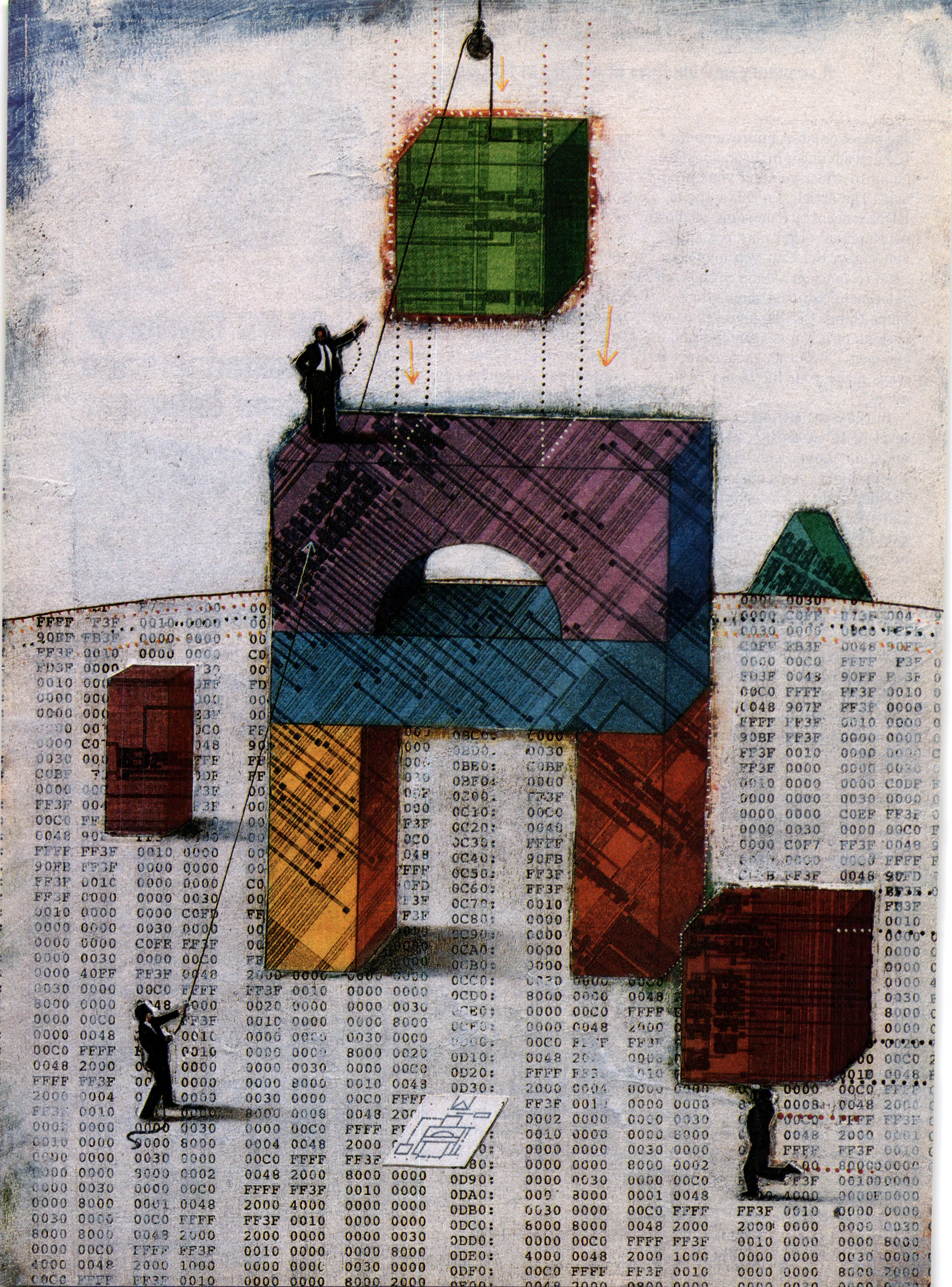
John Gallant's Technology Update on **low-power µPs** looks at the power-management ICs that help you extend battery life in your portable application. "In the late 80s and early 90s, a trend emerged toward putting power equivalent to a desktop PC in portable applications. To do that, you have to be very clever about how you conserve power," says John. "Handheld communicators that keep you in constant contact with home and office is just right around the corner." With that in mind, John gives a survey of popular low-power processors for battery applications and the power-management techniques that will help make personal communicators a reality.

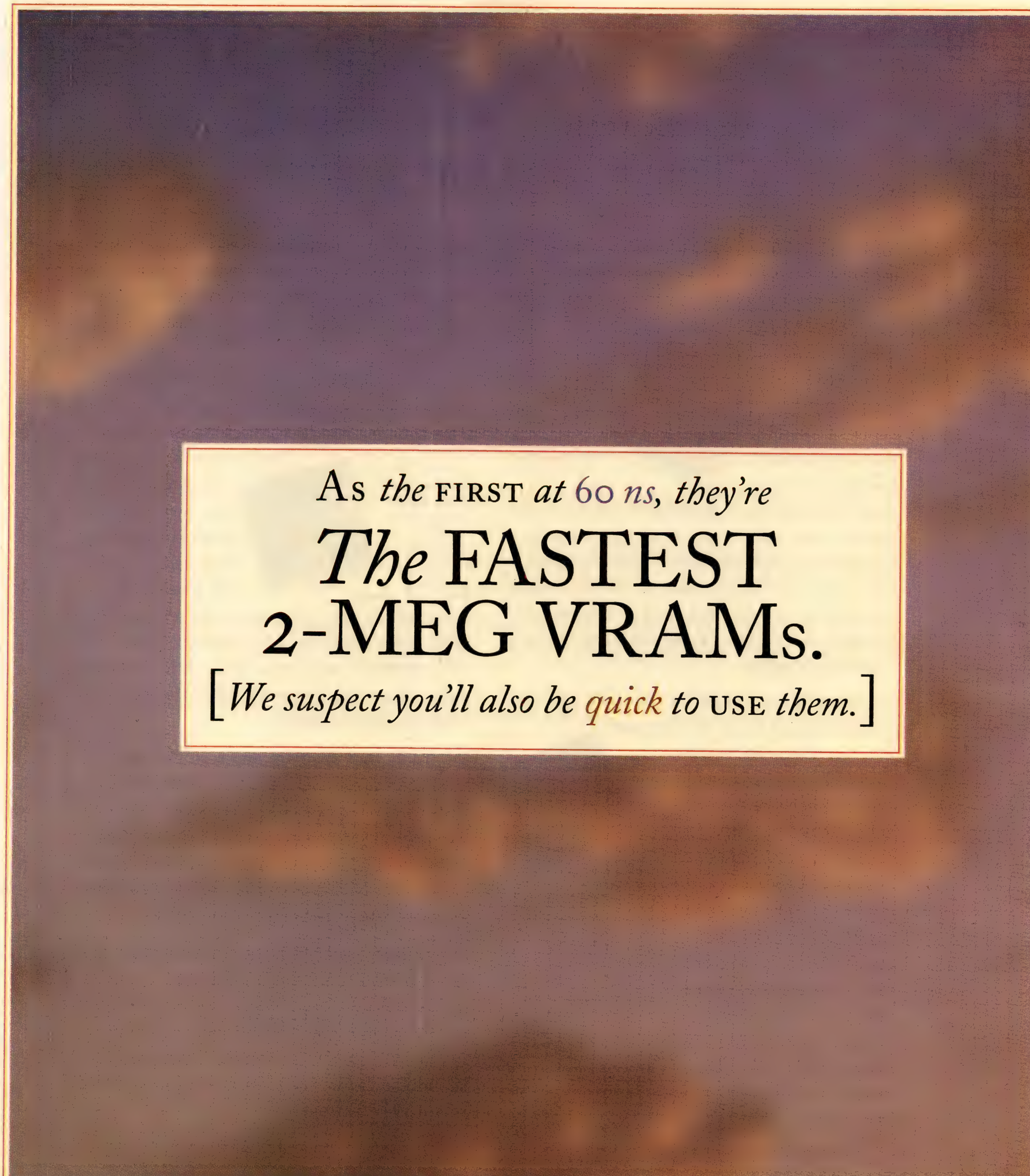
In our Design Features, EDN looks to experts in the field to give insight into other trends. Dave Peters and Jeff Harth of Silicon Systems Inc discuss how **ICs provide control for sensorless dc motors.** Sensorless dc motors are replacing the Hall-effect sensors normally used for motor control. These small, inexpensive, and reliable motors particularly suit rotating-memory, process-control, VCR, fan-motor, heat-pump, environmental-control, robotics, automotive, and toy applications.

Bill Salibrici of TeleSciences Co Systems explores **more uses for DSP chips** in his article. He discuss how you can use a 16-bit fixed-point DSP chip to generate real-time, pseudorandom uniform- or Gaussian-distributed noise signals. These signals can be useful in testing digital filters, in implementing tone detection, in spectral estimation, or for speech-synthesis functions, as well as many other DSP applications.

As the industry changes, so does EDN. EDN is always open to the suggestions of its readers. When we hear an idea we think makes sense, we are happy to implement it. And, if several people suggest something, we figure it's definitely a good idea. Many of you requested reader-service numbers on News Breaks. You've got it. By circling the appropriate number and returning your postage-paid reader-service card to EDN, you will receive free information about the products, trends, and technologies covered in the News Breaks section. Keep the good ideas coming.

Susan Rose
Associate Editor



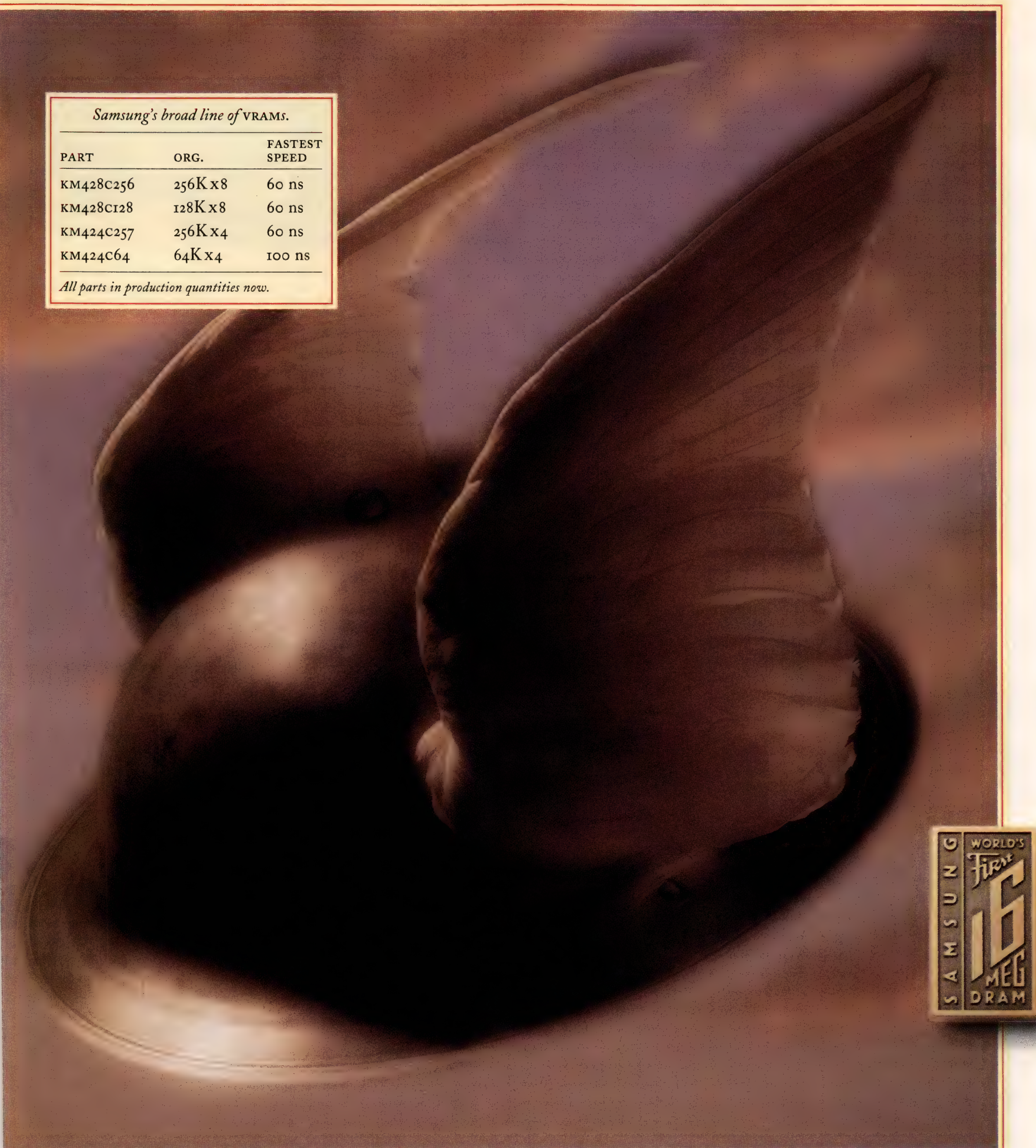


Available in production quantities right now, Samsung's 60 ns, 2-meg VRAM is the fastest in the world. And it's making us one of the leaders in video products.

But it will also do some remarkable things for you. Which means you may want to start putting this extremely fleet VRAM to use in a hurry.

You'll have all the low-parts-count, low-power and low-capacitance advantages of a 2-meg. But you'll also have the advantages of speed—with a 40 ns cycle time for Fast Page Mode, and an 18 ns TSCC. Which will result in faster image creation, and will also make it easier to drive high resolution and high refresh rates.

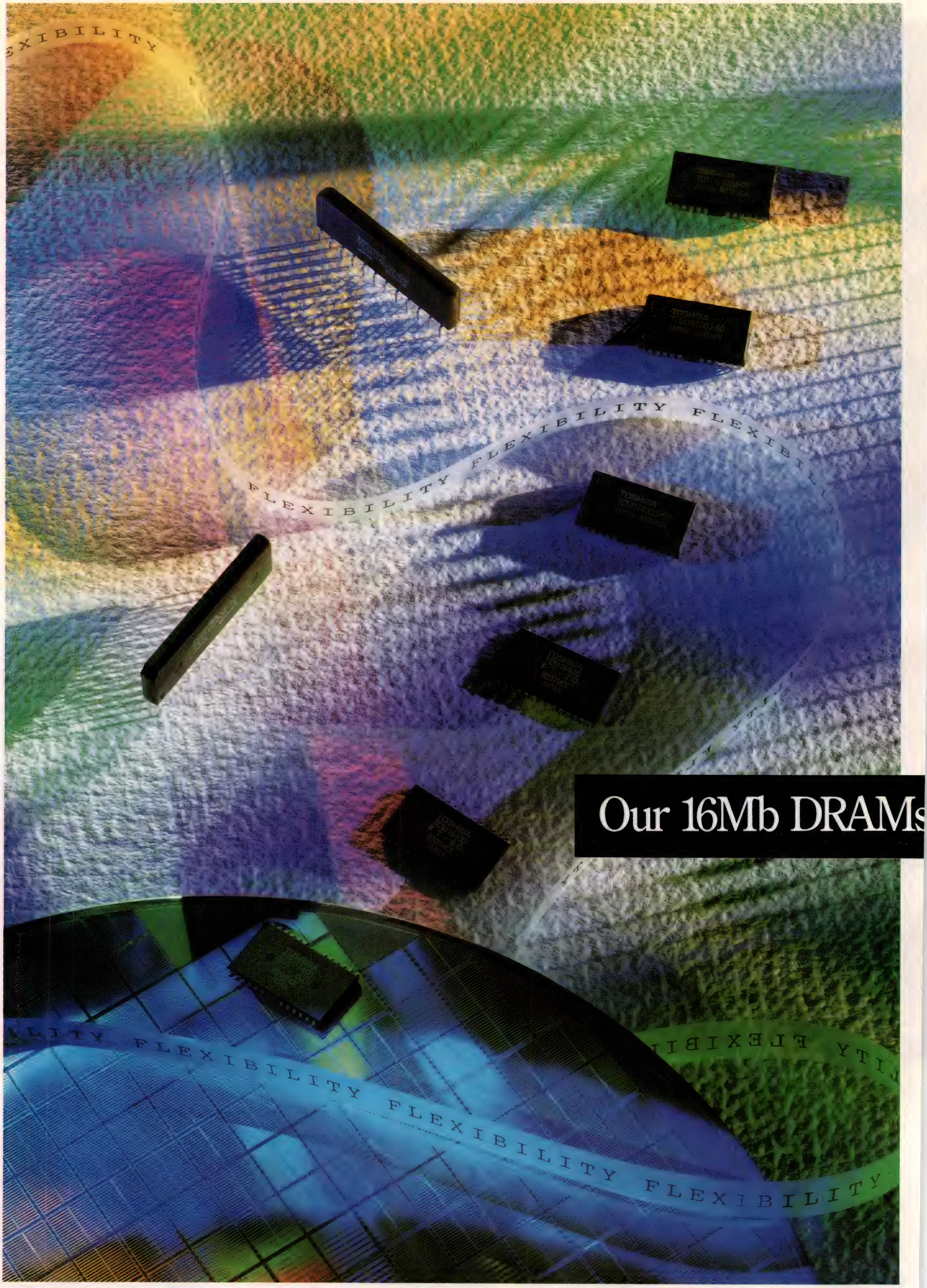
Those things, in turn, will



Samsung's broad line of VRAMS.

PART	ORG.	FASTEST SPEED
KM428C256	256K x 8	60 ns
KM428C128	128K x 8	60 ns
KM424C257	256K x 4	60 ns
KM424C64	64K x 4	100 ns

All parts in production quantities now.


Our 16Mb DRAMs
FLEXIBILITY FLEXIBILITY FLEXIBILITY
TOSHIBA

go to great widths to offer you design flexibility.

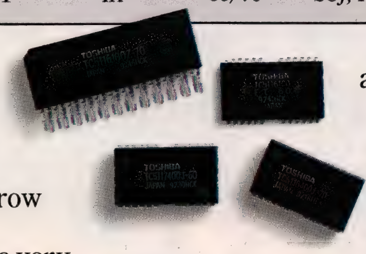
When's the right time to cross over from 4Mb to 16Mb DRAMs?

When you can get access times as quick as 60ns, a greater than four-fold drop in power consumption and greatly increased design flexibility with byte-wide and word-wide organizations— and not a nanosecond sooner.

Or, to put that another way, when you can get a second-generation 16Mb DRAM from that dynamic dynamo, Toshiba. We've combined a 0.55 µm die shrink with optimized row and column architectures. The result: some very compelling reasons to make the move to 16Mb now.

To start with, there's substantial reduction in board real estate when you replace four 1Mx4 parts with one 1Mx16 part. And SIMM modules in 1Mx36 and 2Mx36 configurations, utilizing the 1Mx18 DRAM in place of 4Mb DRAMs, provide elegant solutions in today's power conscious systems.

Organization	*Refresh Rate*	*Access Time (ns)*	*Package*
1MX16	*1K, 4K*	*70/80*	*SOJ, TSOP*
1MX18	*1K*	*70/80*	*SOJ, TSOP*
2MX8	*2K*	*60/70/80*	*SOJ, TSOP*
4MX4	*2K, 4K*	*60/70*	*SOJ, TSOP*
16MX1	*4K*	*60/70*	*SOJ, TSOP*



Our 2Mx8 organizations also give you the cleverest solution for providing 8Mb of base memory in your next generation of portables. And today's higher performance systems can boost system throughput with the wider data paths of 2Mx8, 1Mx16 and 1Mx18 parts.

Combine all this with backward compatibility with the 4Mb generation, access times of 60, 70 and 80ns and wide variety of SOJ and TSOP package options and you end up with maximum design flexibility.

Toshiba is committed to staying at the forefront of memory technology and to keeping you at the forefront of your competitive markets. And we go to great lengths— and widths— to stay on top.

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TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

CIRCLE NO. 116

MST-93-118

EDITED BY SUSAN ROSE

FPGA Update

Programmable-logic performance benchmarks. The Programmable Electronics Performance (Prep) Corp has made the data from its first benchmark suite (version 1.2) of nine circuits available. The benchmarks include data on devices from Actel, Altera, AMD, Cypress, Intel, Quicklogic, Texas Instruments, and Xilinx. The benchmarks show how different field-programmable gate arrays (FPGAs) and complex PLDs compare in speed and capacity for a variety of circuit types. The benchmarks provide a considerable amount of information that should prove helpful to engineers deciding which PLDs are suitable candidates for an application. Certified Prep benchmark results, including background material, cost $25. Prep Corp, Los Gatos, CA, (408) 356-2169, Fax (408) 356-0195. **Circle No. 509**

FPGA software is free and almost free. If you've put off using FPGAs because the high cost of software prevents you from evaluating the devices, your excuses are gone. Intel is now offering the PLDshell Plus 3.0 software for its iFX780 Flexlogic family for free—it previously cost $249. If you currently use Data I/O's Abel or Minc's PLDesigner-XL V3.1, you can obtain free FPGA support by calling (800) 323-3753. Logical Devices CUPL Total Designer V4.4 and Orcad's V2.0 environment also include support for the Intel FPGAs. Intel Corp, Santa Clara, CA, (408) 765-8080. **Circle No. 510**

Quicklogic lets you try out its FPGA design software with a 30-day license and 30-day hotline support for $99. The software includes Windows-based schematic entry, place and route, and full timing analysis. You can view the physical layout of your design and interactively cross-probe between the layout and schematic. The $99 can be applied to the purchase of an unrestricted user license. **Circle No. 511**

FPGA gets faster, cheaper, smaller. Quicklogic has also released a new version of its 1000-gate QL8x12A that is 30% faster, 30% less expensive, and is available now in a 1.4-mm thin quad flatpack (TQFP). The speed increase reduces the logic-cell delays on the fastest versions to 2.4 nsec. You can obtain internal data-path operating speeds of 120 MHz. The price reduction results from a 20% die-size reduction due to a new layout and a move to a high-volume manufacturing facility. The QL8x12A-2 is the fastest version and costs $37.60 in a 68-pin PLCC; the QL8x12A-0 standard-speed version costs $23.20 (1000). The 2000-gate QL12x16 is also available in a TQFP. Quicklogic, Santa Clara, CA, (408) 987-2000, Fax (408) 987-2012. **Circle No. 512**

Ultralow-power FPGA. The Zero+ FPGA family from Xilinx has a 20-μA quiescent current and 5-μA standby current at 3.3V. The XC2014L is available in a 1.1-mm-thick, 64-pin, very thin quad flatpack (VQFP) for $13. The XC3042L, in a 100-pin TQFP, costs $25 (1000).—by Doug Conner. Xilinx Corp, San Jose, CA, (408) 559-7778, Fax (408) 559-7114. **Circle No. 513**

64-Mbit DRAMs arrive

NEC Electronics is now making samples of its 64-Mbit dynamic RAMs (DRAMs) available to designers. The devices are available in 16M×4-bit (μPD42S64400), 8M×8-bit (μPD42S64800), and 4M×16-bit (μPD42S64160) configurations with access times as fast as 50 nsec. The devices use a 3.3V supply and offer a JEDEC-compatible low-voltage TTL (LVTTL) I/O interface. Other features include a self-refresh option and fast page-mode operation. All three configurations are available in thin small-outline packages (TSOP); the μPD42S64400 and μPD42S64800 parts are also available in small-outline J-lead (SOJ) packages. Samples are available, and volume production is scheduled to begin in 1994. High-volume (10,000) pricing starts at $600. —by Richard A Quinnell. NEC Electronics, Mountain View, CA, (415) 965-6000, Fax (415) 965-6130. **Circle No. 514**

PC chip set works with Pentium processor

Designers wanting to turn the Pentium processor into an ISA bus PC now have a chip set available to simplify their task. The 3-chip set includes a bus controller (82C596), a system controller (82C597), and an integrated peripheral controller (82C296). The bus controller serves as a buffer to steer data between the CPU and memory buses, adds parity generation and detection logic, and translates commands between the ISA bus and the VESA local bus. The system controller handles CPU-interface, secondary-cache, and DRAM control. It also interprets and translates bus cycles from the CPU, local-bus master, ISA bus master, and DMA to the host memory, local-bus slave, and ISA bus devices. You can use a system clock as fast as 66 MHz (1×).

The set will work with SRAM to provide a secondary cache for the Pentium. The secondary cache has a direct-mapped, write-back architecture, and its size

Continued on pg 18

SHORTS

Slide rules, anyone? If you're interested in the history of slide rules, or in collecting and preserving them, there's a society just for you. Members receive a semiannual newsletter and swap lists. Membership is $20/year in the US, $25 elsewhere. Osborne Price, 8338 Colombard Ct, San Jose, CA 95135.—JT. **Circle No. 524**

For EE instructors only. Dr David Middlebrook of California Institute of Technology in Pasadena, CA, offers a summer workshop for instructors that trains them how to teach students design-oriented analysis. (If you're not an instructor, there are seminars for you, too.) The Design-oriented Analysis workshop for instructors costs $200 and takes place June 14 to 16 at the Kellogg Center for Continuing Education in Pomona, CA. If you're a circuit designer, ask about the 3-day seminars set for September. Dr Middlebrook, (818) 356-4822—JT. **Circle No. 516**

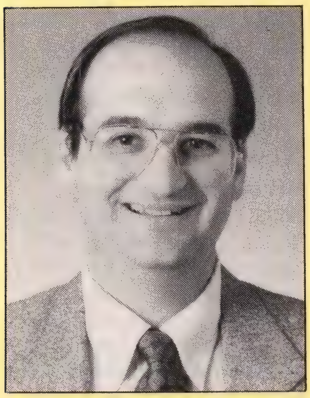
Guide for PC chip sets. The $139 *Personal Computer Design Guide: A Survey of Integrated Solutions*, by Scott Hopkinson provides an approach to understanding PC design and the technical factors that drive a design. The guide covers 255 chip sets from 30 manufacturers.—RW. Annabooks, San Diego, CA, (619) 673-0870. **Circle No. 517**

HP offers symposium. HP's 1993 High-Speed Digital Symposium addresses clock-distribution networks, timing-margin verification, and managing signal-integrity effects. The symposium is free and runs in various cities from April 20 to June 8. Phone HP for scheduling and registration information.—JL. Hewlett-Packard Co, Palo Alto, CA, (800) 765-9200. **Circle No. 518**

Continued from pg 17
ranges from 64 kbytes to 2 Mbytes. The set also has a built-in DRAM controller for as many as four banks of 64-bit-wide page-mode DRAM. The DRAM density can range from 256 kbytes to 8 Mbytes in configurations as large as 128 Mbytes. Sample chip sets, design kits, and technical support are available now. The chip set costs $75 (1000); volume production is scheduled for mid-year. —by Richard A Quinnell. Opti Inc, Santa Clara, CA, (408) 980-8178, Fax (408) 980-8860.
Circle No. 515

Steven H Leibson becomes EDN's Chief Editor

Steven H Leibson has been promoted to Chief Editor of EDN Magazine. Jon Titus, who has held the dual title of Chief Editor and Editorial Director since 1989, will now concentrate solely on his Editorial Director duties. "Steve has done an outstanding job as executive editor during the last year and half. It's a pleasure to have him take over, and both of us look forward to continuing our work together," said Titus. Leibson is now in charge of the day-to-day operations of the magazine edition, freeing Titus to oversee the operations of all of EDN's properties (EDN Magazine, Products and Careers, and EDN Asia) as well as working on other EDN ventures.
—by Susan Rose



Steven H Leibson, EDN's new Chief Editor

New fuzzy-logic processor costs $2

The anticipated movement of fuzzy logic into consumer products may soon become a reality. American Neuralogix Inc is developing a fuzzy-logic processor that will sell for only $2 (100,000). Slated for delivery in September, the NLX-220 processor is suited for products and applications including motor controllers, AGC controllers, power and battery management, smart appliances, security systems, and industrial control.

The chip does not need a host processor or peripheral chips. It has four analog input pins and four analog output pins; other pins provide power, ground, reset/standby, and frequency control for an on-chip oscillator circuit. The device can process 100 input terms and 50 rules. It provides six selectable membership functions in mask ROM. Parameters for fuzzy-logic rules that you specify also go into mask ROM. Smaller quantities of the chip will be available but will include a mask-ROM charge. In quantities of 1000, for example, you'll pay $5.25 per chip plus a mask fee of $7000.
—by Gary Legg. American Neuralogix Inc, Sanford, FL, (407) 322-5608.
Circle No. 519

Templates speed power-electronics designs

Power Express from Analogy is a power-electronics design and analysis package that speeds design by offering topology templates. The templates are part schematic and part system models of popular power-electronic topologies used in power supplies, motor-drive circuits, and power-factor-correction circuits. The models are predefined and presimulated, which lets you quickly evaluate multiple configurations to determine the best one to meet your design requirements. Templates offered in the initial release include buck, boost, buck-boost, cuk, sepic, zeta, forward flyback, push-pull, full bridge, and half bridge. The package will be available as a $5000 option to Saber. Bundled with Saber, prices start at $30,000. The software runs on Sun and HP workstations. —by Doug Conner. Analogy, Beaverton, OR, (503) 626-9700, Fax (503) 643-3361. **Circle No. 520**

Circuit board emulates ASICs

A field-programmable circuit board from Aptix works in conjunction with software from Pie Design Systems to emulate ASICs with up to 30,000 gates. The FPCB-AP4 has sockets to accommodate up to 16 Xilinx 4010 FPGAs and four field-programmable interconnect devices from Aptix. A 320-pin prototyping area lets you add RAM and other hardware to expand the system's capacity beyond 30,000 gates. Although speed depends on the application, the company expects most applications to run at clock speeds of 10 to 20 MHz. Pie Design Systems provides the Mars compiler software necessary to automatically partition and map designs into the board.

A fully configured system costs $60,000, including software and a fully populated programmable circuit board. Once you've finalized a design, you can purchase replicate boards that have all configuration data stored in nonvolatile memory. The replicate boards are useful for hardware and software development after you've finalized the design and before you have working ASICs from your foundry. Replicate boards cost $25,000. The field-programmable circuit boards are available now; the Mars compiler software will be available in the third quarter of 1993. —by Doug Conner. Aptix Corp, San Jose, CA, (408) 428-6200, Fax (408) 944-0646. **Circle No. 521**
Pie Design Systems, Sunnyvale, CA, (408) 738-8899, Fax (408) 738-8853. **Circle No. 522**

Placement drives ASIC logic synthesis

To meet high-density ASIC needs, Cadence Design Systems has added placement-based synthesis to its Synergy PBS (Placement-Based Synthesis) design tool. The package makes a preplacement pass on the finished netlist before the silicon layout/verification phase. The tool rearranges the netlist to reduce interconnect. Additionally, it resizes gates and buffers based on layout and inserts new gates as needed to reduce overall timing delays. The resulting optimized netlist is then passed to standard ASIC place-and-route tools to finalize the ASIC's silicon. The company claims that by including preplacement in the design cycle, timing performance improves 10 to 30%, depending on the design.

Enhanced Synergy, with placement-based logic synthesis, will be available this quarter; it costs $55,000 and includes a VHDL or Verilog Synthesizer/Optimizer. The Synergy PBS option is available for $25,000. —by Ray Weiss. Cadence Design Systems Inc, San Jose, CA, (408) 943-1234. **Circle No. 523**

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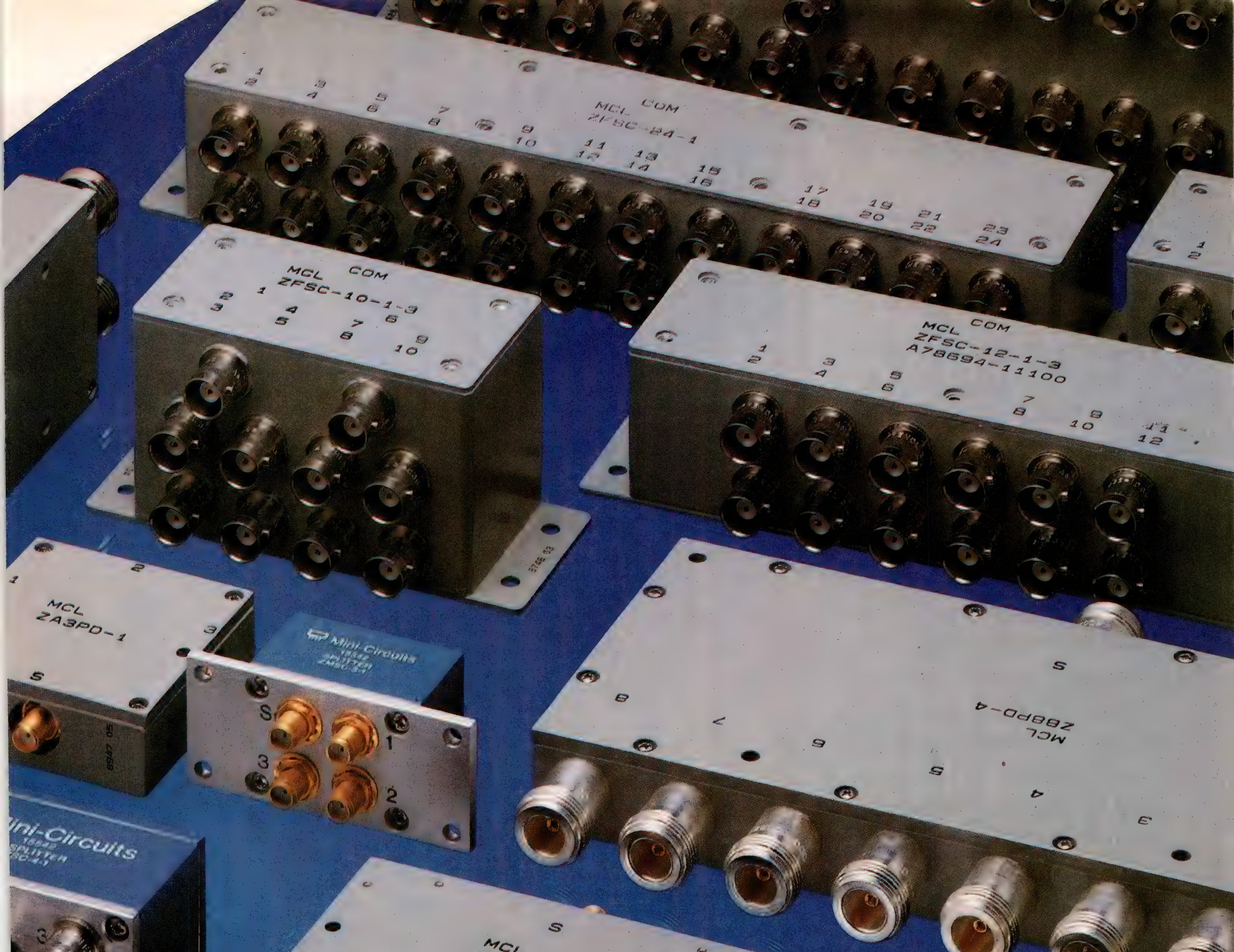
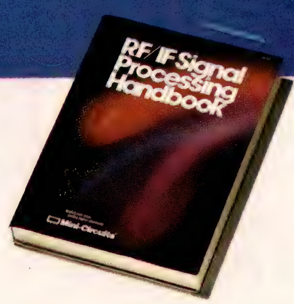
F134 REV. C





For detailed specs on all Mini-Circuits products refer to
• THOMAS REGISTER Vol. 23 • MICROWAVES PRODUCT DIRECTORY
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CIRCLE NO. 74

F134 REV. C

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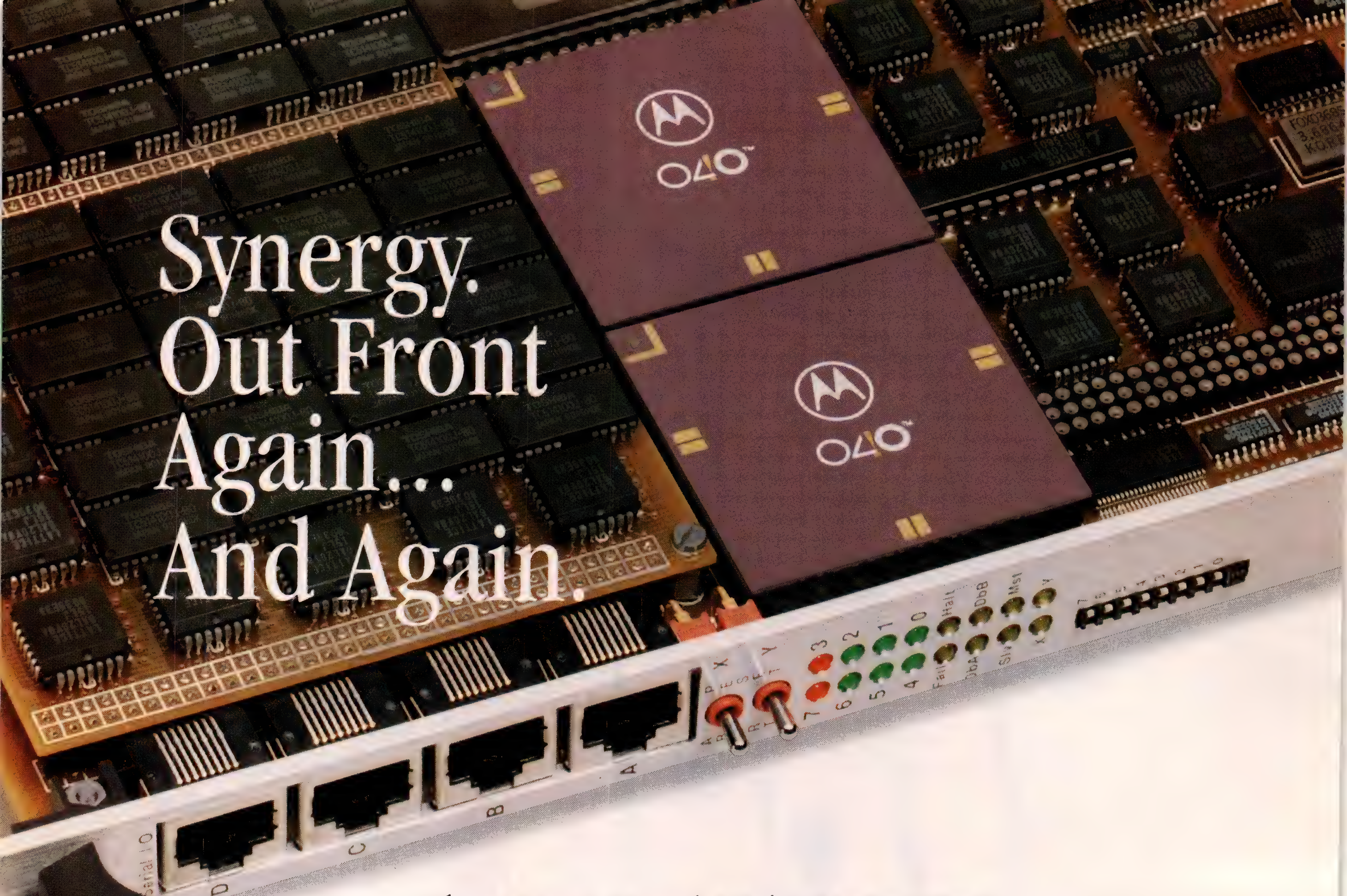
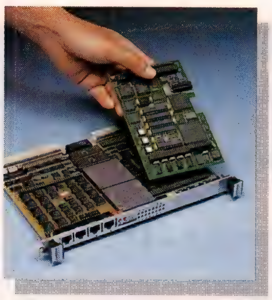


The New Dual '040 VME SBC: Faster, More Efficient and Lower Cost Than Any Multi-board Solution

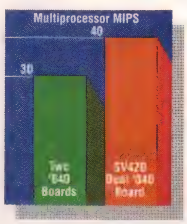
Get on-board multiprocessing and an astounding **40 MIPS** throughput, when you power your system with Synergy's new SV420 single-slot SBC. The SV420's dual-CPU design means you'll need fewer boards in your VME chassis, with no VMEbus bandwidth bottlenecks between the '040s, and system-wide cost saving of more than 40%.

And even if you don't need multiprocessing right now, the SV420 still puts you out front. Use the second '040 as a super-smart DMA controller. When combined with the SV420's **66 MByte/sec** VME64® circuitry, nothing communicates faster over the VMEbus.



Over a dozen smart, powerful I/O modules fit Synergy's '020, '030, '040 and Dual '040 SBC's.

Add even more on-board power by selecting from Synergy's big list of high-performance, intelligent plug-on I/O modules – such as our latest Super-VSB module offering 40+ MB/sec over the VSB bus. Or choose another module, from a T1/E1 controller to a super-fast graphics engine, that plugs onto any Synergy SBC.



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CIRCLE NO. 66

EDITED BY JULIE ANNE SCHOFIELD

Reader needs EPROM, contents, or firmware program

My company is searching for the firmware program listing, EPROM contents, or actual 2708 EPROMs for the National Semiconductor BLC 8229/8228 CRT/keyboard controller. These devices were also part of the company's Starplex development system. National no longer supports the Starplex system, nor could it recommend a company that does. Is there anyone out there from whom we can beg, borrow, or buy any of these devices?
L Mente
Software Engineer
Amparts Electric
South Holland, IL

Let's find out.

Zero-crossing detector may not be the problem

I am in dire need for quick information on using a zero-crossing or peak detector with the minimum amount of parts to interface with a Z-World Z180 microcontroller in an embedded system. "The Computer Applications Journal" (February 1993) suggested the ac power line as an excellent time base. You derive that time base using an optoisolator and a 74IS14 as a zero-crossing detector. We're swamped with putting our resources into coding and don't have a lot of time for this circuit. We tried sampling the 10-bit ADC more frequently than we did in an earlier project, but this tack took about 25% of our processor time to get the accuracy (100ths of the power-line frequency) we need. We catch the volts and amps at the crossing and use the timestamps to calculate power factor and frequency. I am under the gun and responsible for both the hardware microcontroller interface to our machine as well as the bulk of the coding. Could you drop me a hint or two and help pull off an eleventh-hour miracle?
Mike Raffesberger
Intelligen
San Marcos, CA

The Cahners CAPS (Computer-Aided Product Selection) System from Cahners Technical Information Services (Newton, MA) coughed up only one "zero-crossing" chip: Siemens's IL426. That chip is a 600V 2A power triac—probably not what you want. You can call Siemens Components (Santa Clara, CA) at (408) 980-4518, or fax them your request at (408) 980-0319.

A scan of the Design Idea files yielded the following DIs that feature zero-crossing detectors, as well as the EDN issues they appeared in: "Power controller switches cycles" (3/15/90, pg 179), "VFC rejects common-mode noise" (1/21/91, pg 166), "Current loop controls SCRs" (2/4/91, pg 106), "Phase shifter adapts to frequency changes" (6/6/91, pg 184), and "Single-chip μP suppresses unwanted tone" (12/5/91, pg 196). For other zero-crossing circuits, see the *IC Op-Amp Cookbook*, by Walter Jung (Howard W Sams & Co, Indianapolis, IN) and *The Art of Electronics*, by Paul Horowitz and Winfield Hill (Cambridge University Press, New York, NY).

Frankly, we don't understand how you could be chewing up 25% of your μC's time measuring something that happens 120 times/sec. How about letting a counter run free at whatever rate will give you the resolution you need? You could use the output from the zero-crossing detector as an interrupt to store the current counter value into a register or memory location. Some simple math that accounts for counter overflow should yield the difference between two successive readings. In other words, perhaps your computational algorithm is your real problem, not a zero-crossing detector circuit. If you're out of internal counters, try using an external one.

Data-analysis software is a bargain compared with stand-alone instrument

I've been searching for data-analysis-type software that would write all data both passed by modem and running in a program to the screen, so I could watch data flowing in both directions via a split window. I have heard of such programs but don't remember a program or author name. Can you help?
Howard Lukenbill
HSL Inc
Pueblo, CO

Try the program Microtap (formerly Datascope). It costs $299, including the special cabling you'll need. Serial-data analyzers start at $10,000 as stand-alone instruments, so the software is quite inexpensive.

Paladin Software Inc
3945 Kenosha Ave
San Diego, CA 92117
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Fax (619) 490-0177

Spice source code not available in Fortran

I need a point of contact for Berkeley Spice Fortran source code. Our government customer wants to upgrade a mainframe-based Spice front end to a microprocessor-based tool. I understand that Spice is available to the government in source form for a nominal price, but I need a phone number to call.
Bill Hensley
TRW
Midwest City, OK

Bad news, Bill. The folks at Berkeley gave up on Fortran and recoded Spice in C. Hope you have a C compiler. Berkeley sells Spice to anybody—not just institutions—for a media fee. Contact

Industrial Liaison Program
Software Distribution Office
Department of Electrical Engineering and Computer Science
Electronics Research Lab
205 Cory Hall
University of California, Berkeley
Berkeley, CA 94726
(510) 643-6687.

Also, it wouldn't hurt to get yourself a postprocessor to turn number-stuffed Spice files into graphs and to do things like Fourier transforms. Look on the EDN BBS's /SPICE Special Interest Group for the TRSpice postings.

Ask EDN solves nagging design problems and provides the answers to difficult questions. Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. Fax (617) 558-4470; MCI: EDNPRIME. Or, send us a letter on EDN's bulletin-board system at (617) 558-4241, 300/1200/2400 8,N,1. From the Main System Menu, enter ss/ask_edn and select W to write us a letter.

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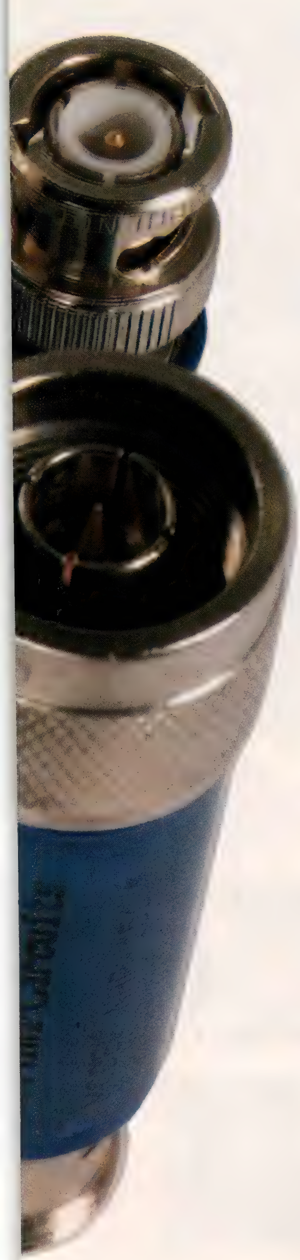
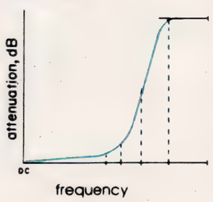
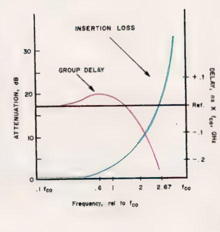
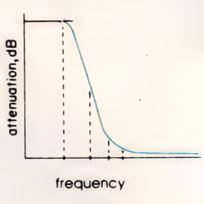


LOW PASS

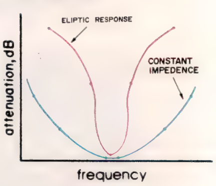




HIGH PASS



BANDPASS



low pass, Plug-in, dc to 1200MHz

Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
★LP-5	DC-5	8-10	10-200
★LP-10.7	DC-11	19-24	24-200
★LP-21.4	DC-22	32-41	41-200
★LP-30	DC-32	47-61	61-200
★LP-50	DC-48	70-90	90-200
★LP-70	DC-60	90-117	117-300
★P-90	DC-81	121-137	167-400
★LP-100	DC-98	146-189	189-400
★LP-150	DC-140	210-300	300-600
★LP-200	DC-190	290-390	390-800

Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	Stopband, MHz loss > 40dB
★LP-250	DC-225	320-400	400-1200
★LP-300	DC-270	410-550	550-1200
★LP-450	DC-400	580-750	750-1800
★LP-550	DC-520	750-920	920-2000
★LP-600	DC-680	840-1120	1120-2000
★LP-750	DC-700	1000-1300	1300-2000
★LP-800	DC-720	1080-1400	1400-2000
★LP-850	DC-760	1100-1400	1400-2000
★LP-1000	DC-900	1340-1750	1750-2000
★LP-1200	DC-1000	1620-2100	2100-2500

Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $35.95

Surface-mount, dc to 570MHz

SCLF-21.4	DC-22	32-41	41-200
SCLF-30	DC-30	47-61	61-200
SCLF-45	DC-45	70-90	90-200
SCLF-135	DC-135	210-300	300-600
SCLF-190	DC-190	290-390	390-800
SCLF-380	DC-380	580-750	750-1800
SCLF-420	DC-420	750-920	920-2000

Price, (1-9 qty), all models: $11.45

Flat Time Delay, dc to 1870MHz

Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	Stopband MHz loss > 20dB	VSWR Freq. Range, DC thru 0.2fco $\bar{X}$	VSWR Freq. Range, DC thru 0.6fco $\bar{X}$	Group Delay Variations, ns Freq. Range, DC thru fco $\bar{X}$	2fco $\bar{X}$	2.67fco $\bar{X}$
★BLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0
★BLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9
★BLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5
★BLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6
★BLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8
★BLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15

Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.

high pass, Plug-in, 27.5 to 2200MHz

Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband, MHz loss < 1dB	VSWR Pass-band Typ.
★HP-25	DC-13	13-19	27.5-200	1.8:1
★HP-50	DC-20	20-26	41-200	1.5:1
★HP-100	DC-40	40-55	90-400	1.8:1
★HP-150	DC-70	70-95	133-600	1.8:1
★HP-175	DC-70	70-105	160-800	1.5:1
★HP-200	DC-90	90-116	185-800	1.6:1
★HP-250	DC-100	100-150	225-1200	1.3:1
★HP-300	DC-145	145-170	290-1200	1.7:1

Model No.	Stopband MHz loss < 40dB	Stopband MHz loss < 20dB	Passband, MHz loss < 1dB	VSWR Pass-band Typ.
★HP-400	DC-210	210-290	395-1600	1.7:1
★HP-500	DC-280	280-365	500-1600	1.8:1
★HP-600	DC-350	350-440	600-1600	2.0:1
★HP-700	DC-400	400-520	700-1800	1.6:1
★HP-800	DC-445	445-570	780-2000	2.1:1
★HP-900	DC-520	520-660	910-2100	1.8:1
★HP-1000	DC-550	550-720	1000-2200	1.9:1

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

bandpass, Elliptic Response, 10.7 to 70MHz

Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands I.L. > 20dB at MHz	Stopbands I.L. > 35dB at MHz
★BP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
★BP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
★BP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
★BP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
★BP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in $18.95,
BNC $40.95, SMA $42.95, Type N $43.95

Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
★IF-21.4	21.4	18-25	1.3 & 150	DC-220
★IF-30	30	25-35	1.9 & 210	DC-330
★IF-40	42	35-49	2.6 & 300	DC-400
★IF-50	50	41-58	3.1 & 350	DC-440
★IF-60	60	50-70	3.8 & 400	DC-500
★IF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in $14.95,
BNC $36.95, SMA $38.95, Type N $39.95

NOTE: ★**Add Prefix P, B, N, or S for Pin, BNC, N, or SMA connector requirement.**

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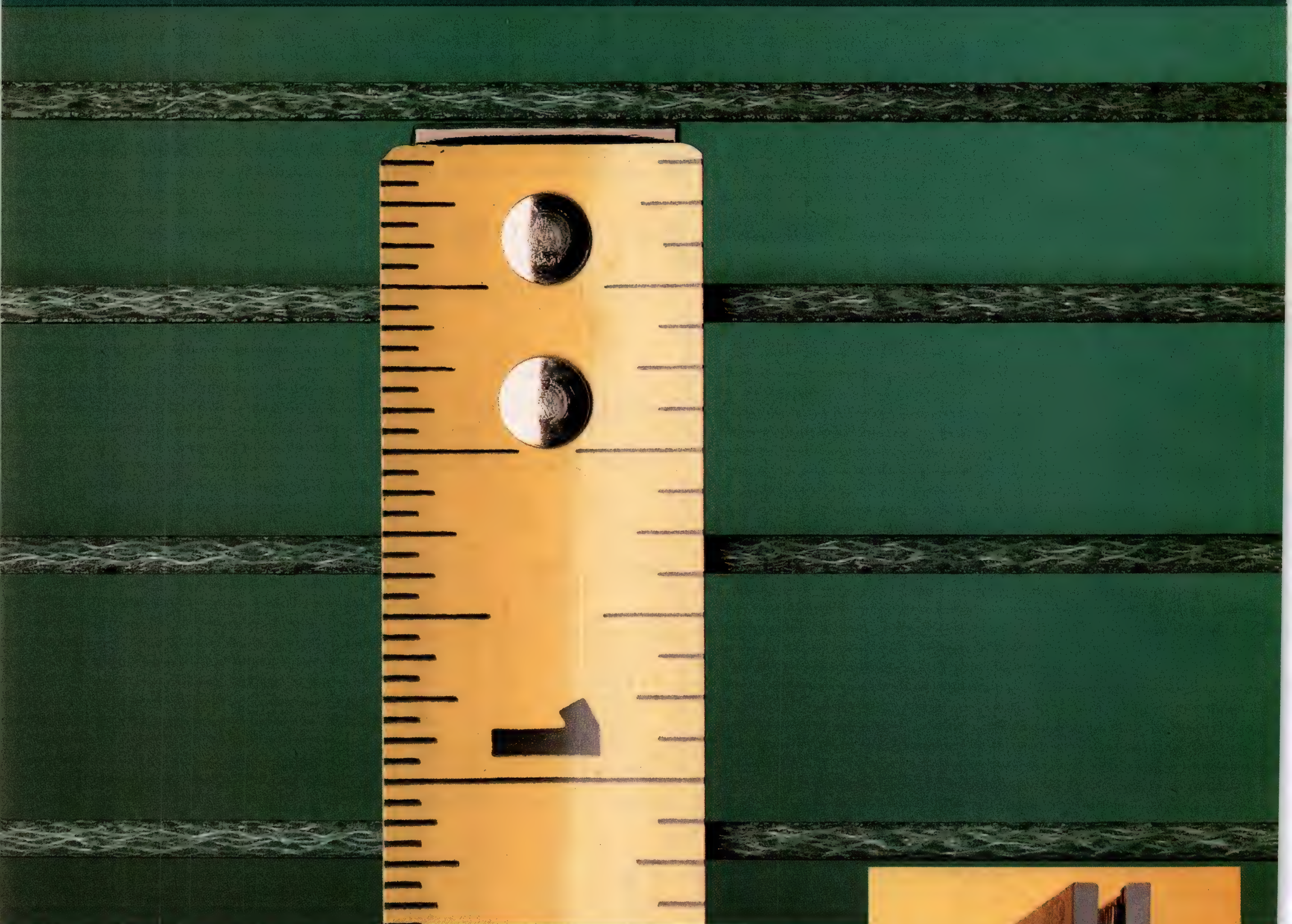
F132 REV. C

.050 centerline stackers. Close, closer, closest.



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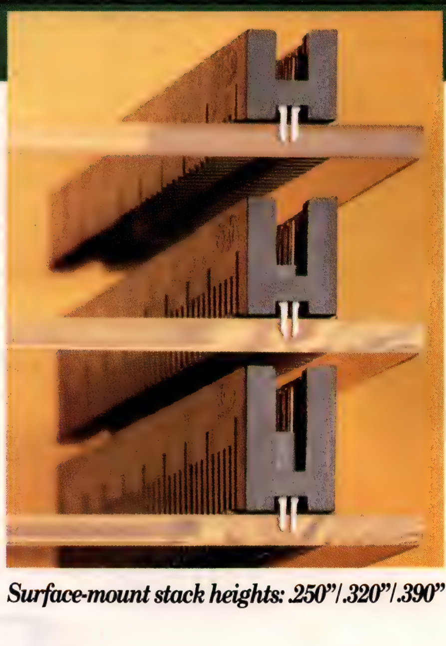
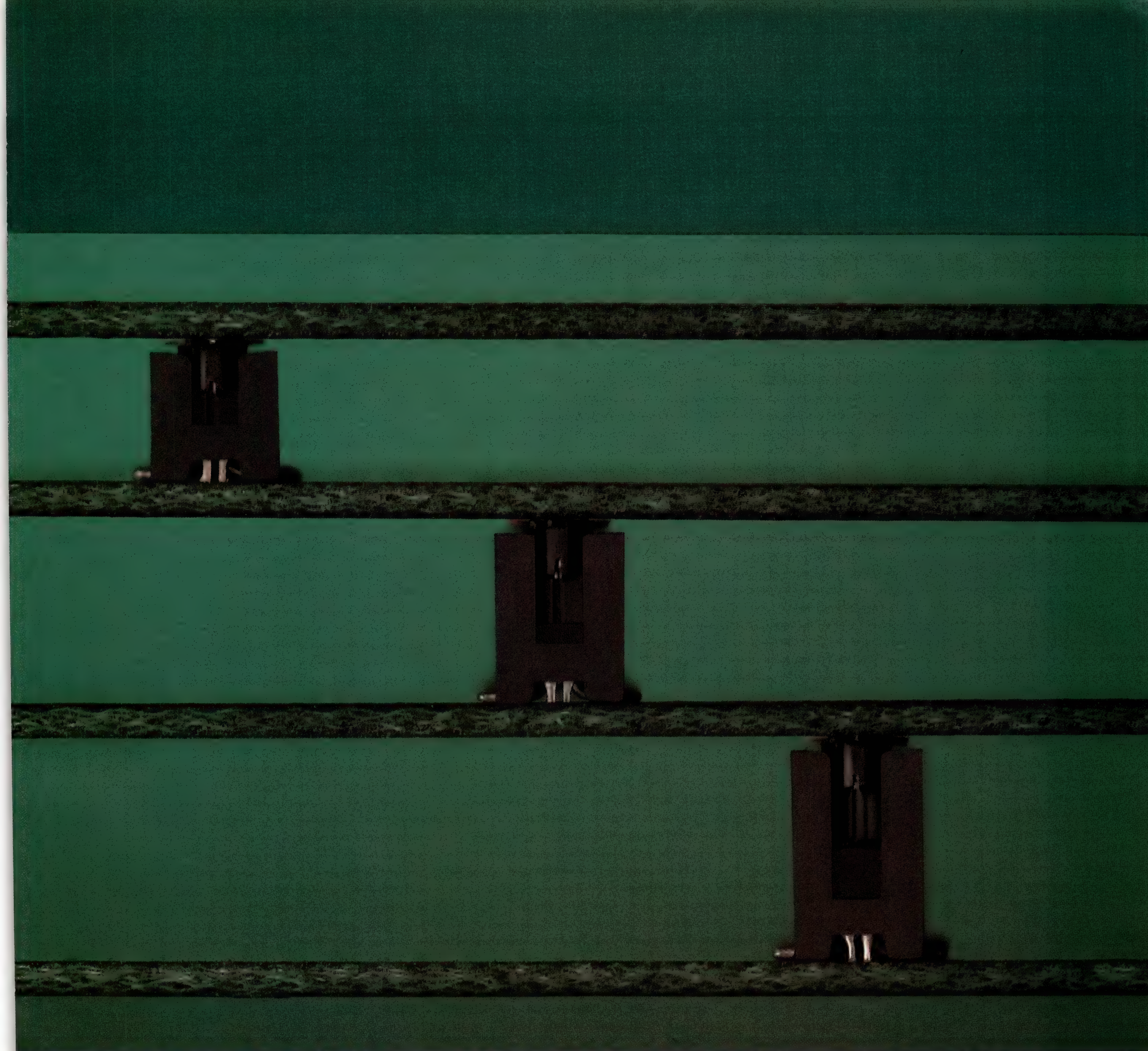


Surface-mount stack heights: .250"/.320"/.390"



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France 1-34 43 27 20 (fax 1-3030 4550)

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AMP

CIRCLE NO. 17

No policy is good policy

Now that the US has a Democratic administration, we again face the debate about whether we need a national industrial policy. It's interesting that many of our high-tech corporate executives are lining up to tout the virtues of industrial policy. Many of these same people would be peddling potato chips if the US had put an industrial policy in place years ago. Past industrial policies might have included statements such as, "The future is in mainframes, no one will want their own small computers." Or how about, "Microprocessors are toys, the future belongs to minicomputers." Of course, these policies never existed, but they might have. Luckily, the bureaucrats were kept out of policy making for the electronics industry. As the US again debates the need for an industrial policy, here are a few things to consider:

In the 1960s, many European countries and companies, alarmed at the growing military-industrial complex in the US, demanded industrial policies and joint industrial-government ventures. What they got were large bureaucratic money pits that continue to lose technology, market share, and market battles. A European consortium continues to spend billions of dollars on an obsolete HDTV proposal.

Japan's Ministry of International Trade and Industry (MITI) continues to scare US electronics industries. For example, MITI sponsored millions of dollars of research into the fifth-generation computer, and a cry went out in the US that we must have a similar project, too. But today that approach is uncompetitive, and even US supercomputer companies are having a difficult time. That's what competition is supposed to be all about. Now, name a MITI success. You can't; there aren't any that count.

The US already has many government policies. For example, we have a farm policy that subsidizes unprofitable, uncompetitive farms. We hear cries that we must preserve the small family farms. Why? Did we preserve the small neighborhood bakeries and candlemakers? No, and with good reason—they couldn't compete.

The US pays people to not produce food. When they produce too much, the US government buys it and stores it, thus keeping food costs artificially high. The stored food usually doesn't go to people who could use it. Instead, it spoils. We subsidize our dairy industry with over $400 million per year, and dairy farmers must kill cattle to keep dairy production down. In addition, our farm policy keeps prices for oranges, peanuts, and sugar above what they should be. We subsidize industries to the detriment of consumers.

We have a military policy, too. It means that the US Congress often forces our Department of Defense to buy weapons it doesn't want or need. The policy also means that we maintain military bases that no longer have a purpose.

We have a land-use policy that lets companies "lease" 500 *million* acres of government land for mining, timbering, or grazing. Leasing rates are far below those for privately owned land. In addition, our wetlands policy jails a landowner who fills in a small damp area on his property, yet it lets municipalities and farmers make profligate use of precious and irreplaceable water resources elsewhere.

The US had an alternative-energy policy that spent billions for research into clean fuels, solar energy, energy conservation, wind power, and synthetic fuels. While the goals were admirable, the program was a boondoggle that tried to predict future energy needs and trends. Today we simply import more oil than ever, and conservation is voluntarily undertaken by those who want to pay less for energy. The hidden hand of the market governs what energy we buy and what we conserve.

And, the US has a space and science policy that continues to sink billions of dollars into a space station that has no clear mission and a super-conducting collider that stands to benefit a handful of academic physicists out for Nobel prizes.

I agree, my examples are short and simplistic. But, what was it you wanted to tell me about needing an industrial policy?

Jon Titus

Jon Titus
Editor

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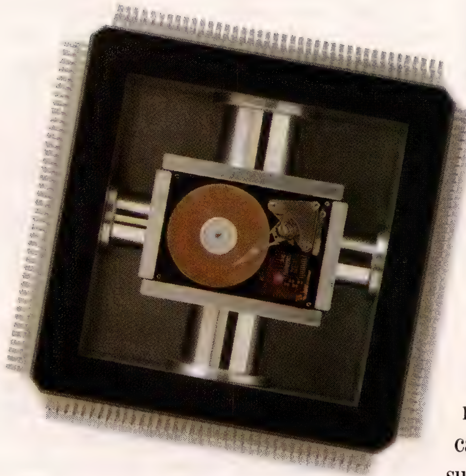

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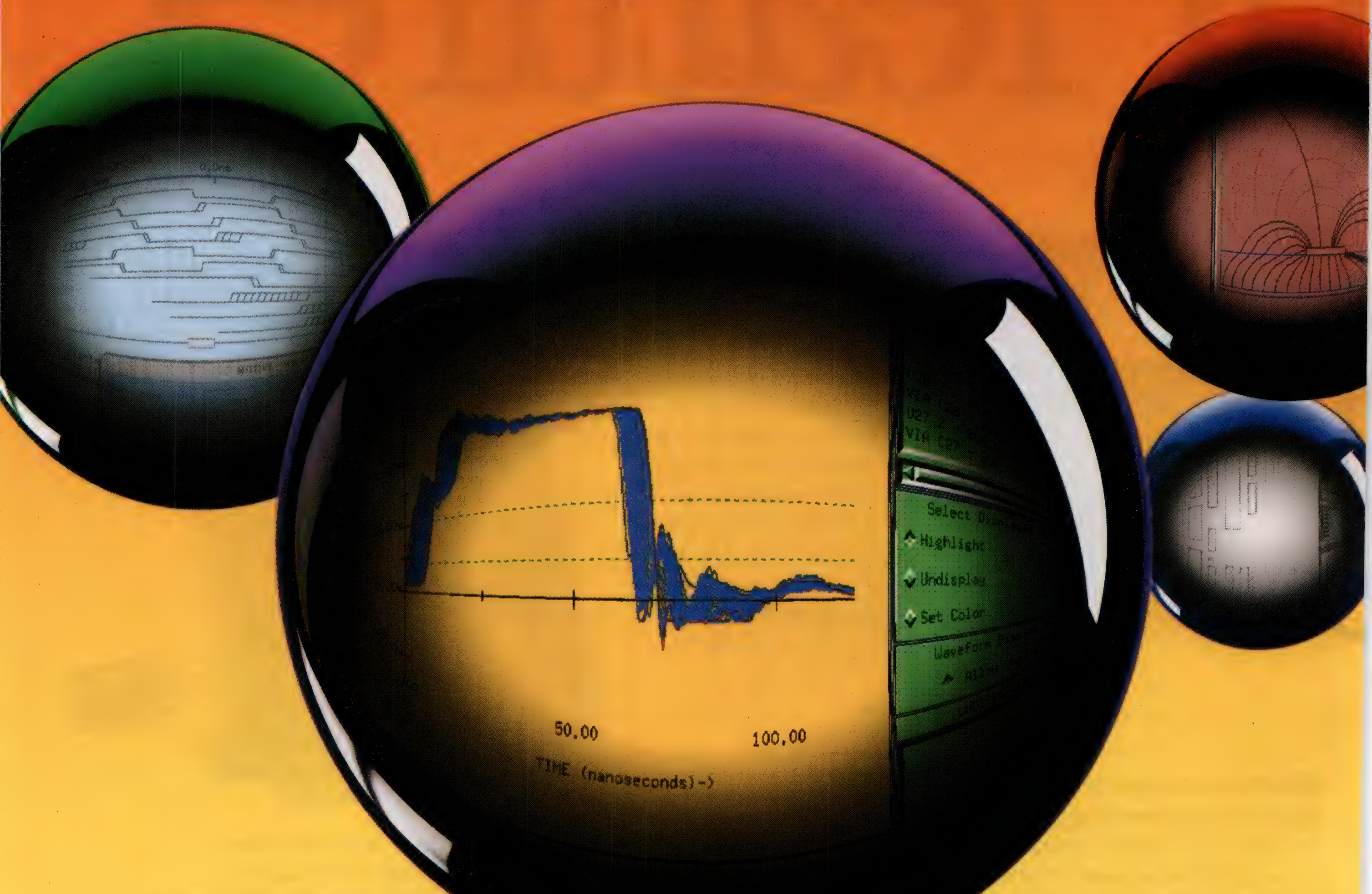

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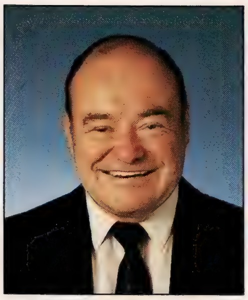
CIRCLE NO. 64

Low-power μPs simplify design of portable computers

JOHN GALLANT, Technical Editor

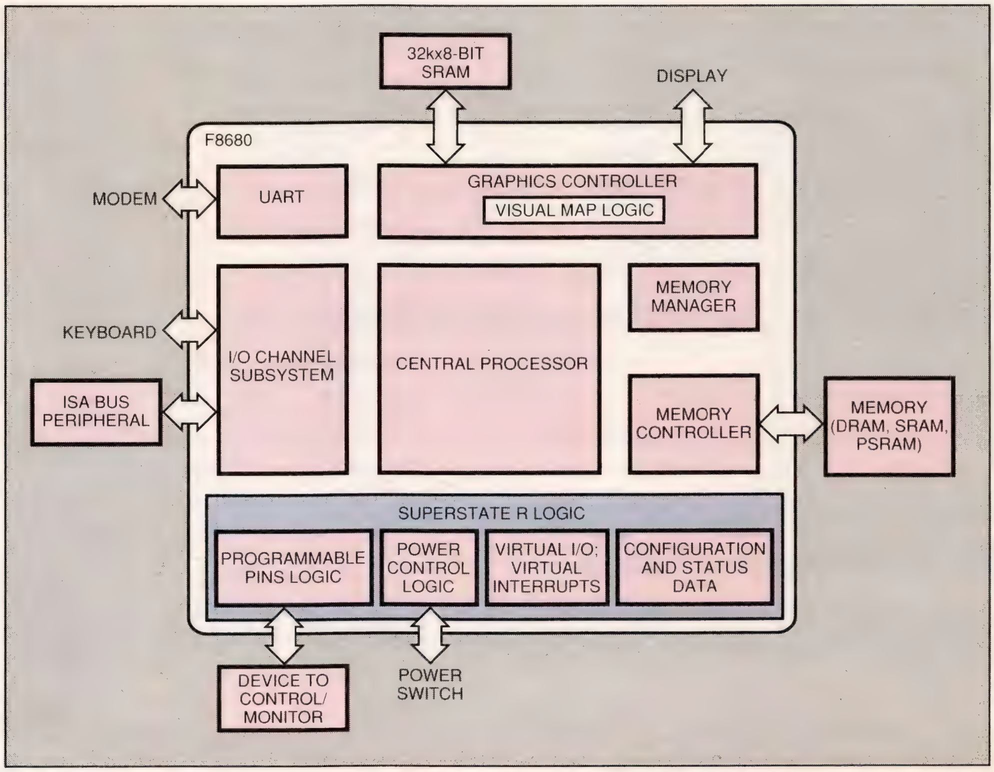


Portable computers are changing the way people do business. At the heart of these compact mobile units are μPs with sophisticated power-management features that conserve battery life.

Designers of first-generation portable computers quickly recognized the need for conserving as much energy as possible from batteries. Because normal operating conditions create battery discharge times of less than 1 hour, portable-computer designers were forced to implement innovative power-savings schemes. In response, microprocessor (μP) vendors have developed a host of μPs for low-power applications using sophisticated power-management techniques. These techniques extend battery life between charges to four hours—or more.

One of the first μPs for low-power applications is the i386 SL, which Intel introduced in 1990 (5V, 25-MHz version, \$66 (1000)). The μP features a 16-, 20-, or 25-MHz i386 core and a power-savings method, called system management mode (SMM), which is transparent to normal operating conditions. To implement SMM, the i386 SL adds two new pins to the i386 CPU. A nonmaskable hardware interrupt, called system management interrupt (SMI), and a CPU acknowledge signal, called SUS-STAT. SMI has a higher priority than the standard nonmaskable interrupt (NMI) for the i386 μP.

Quick on Intel's heels, AMD introduced the 25- and 33-MHz Am386SXLV μP (25-MHz version, \$37 (1000)). This



The Chips and Technologies F8680 PC/Chip runs 8086 opcode, but delivers 80286 performance figures. A SuperState R mode lets you implement transparent power-saving states.

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LOW-POWER µPs

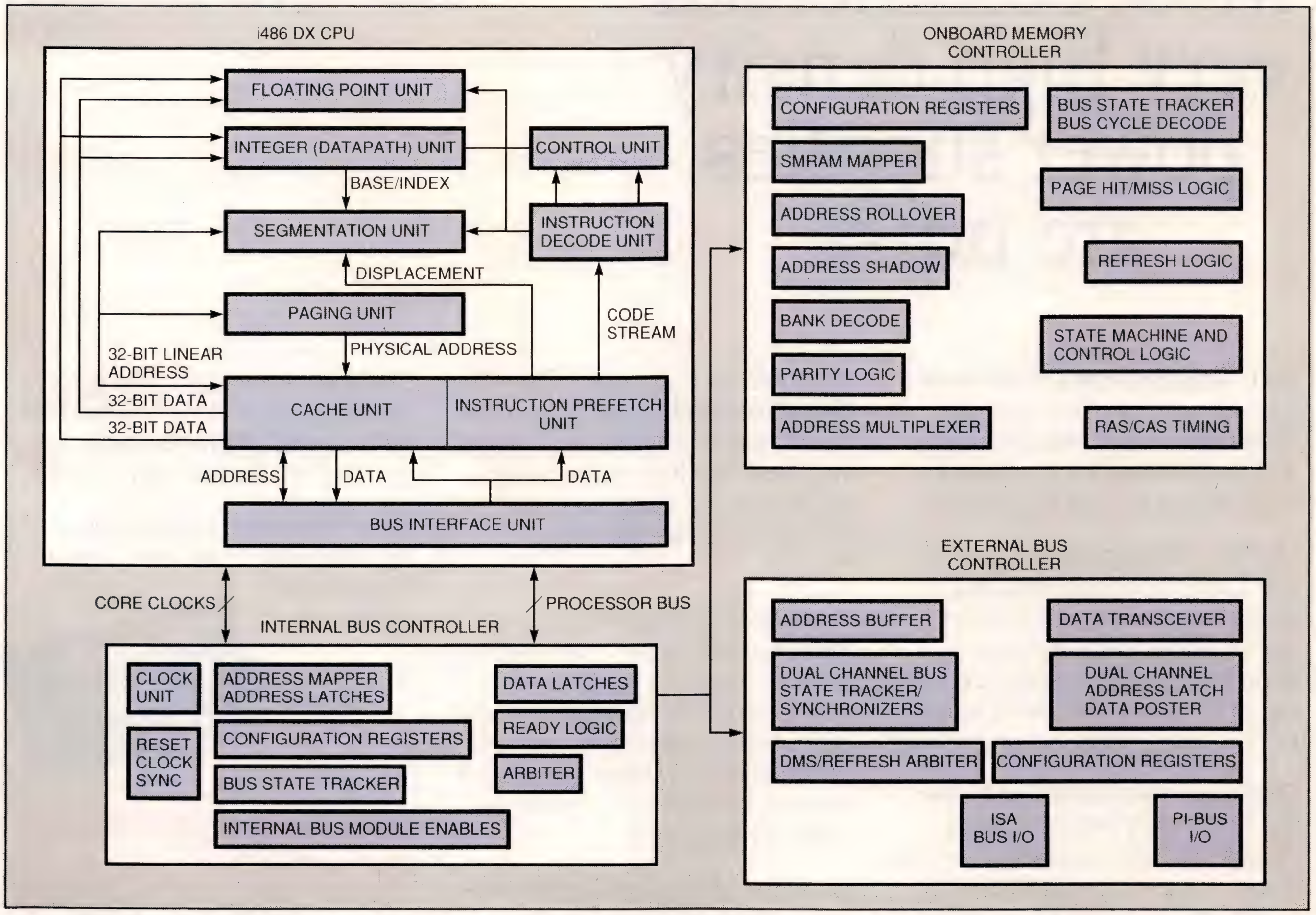
µP is a clone of Intel's i386SX core and has a variation of SMM. In 1992, Cyrix introduced the Cx486-SLC and Cx486DLC µPs. Both µPs run Intel's i486SX instruction set and feature another variation of SMM. At the end of 1992, Cyrix announced a 33-MHz enhanced version of the Cx486SL, called the Cx486SLC/e (25-MHz version, $99 (1000)). Intel also introduced a new low-power µP, the i486 SL (low-voltage, 25-MHz version, $227 (1000)) in the fourth quarter of 1992.

Because the Cx486SLC/e and i486 SL are recent introductions and carry the powerful 486 nomenclature, you can draw some logical comparisons. First, neither processor is simply a low-power version of the i486DX µP. Intel integrated a dynamic RAM (DRAM) controller, a 16-bit ISA bus controller, and a 16-bit parallel interface (PI) bus controller on the i486 SL. The i486 SL runs object code for all 80x86 µPs and comes in a 196-pin plastic quad flatpack (PQFP), 208-pin shrink QFP (SQFP), or 227-pin LGA.

The 25- or 33-MHz i486 SL has a fully static 32-bit i486DX core and an i386 SL-compatible SMM. The core has an enhanced version of the i387 coprocessor and a 4-way, set-associative, 8-kbyte cache. Static registers let you stop the clock to conserve power without losing data. Static designs, which require a minimum clock rate to maintain data, are new to Intel, who previously used dynamic registers in 80x86 designs.

In contrast, the 20-, 25-, or 33-MHz Cx486SLC/e comes in a 100-pin PQFP that has the same footprint as an i386SX µP, which is used in first-generation designs, but executes the i486SX instruction set. Internally, the chip is considerably different compared with the i486 SL. It has a 1-kbyte direct-mapped, or 2-way set-associative instruction and data cache. Instead of an FPU, the chip has a 16-bit hardware multiplier to accelerate graphics or handwriting-recognition algorithms.

The Cx486SLC/e execution unit consists of a 5-stage pipeline, which overlaps code fetches, instruction decoding, microcode ROM accesses, execution, and writes back to memory or register. The RISC-like architecture permits most instructions to run in a single cycle. Although the Cyrix SMM is functionally equivalent to the Intel



The Intel i486 SL µP features a static 3.3V i486DX core and an i386 SL-compatible SMM. A DRAM controller and an ISA and PI bus controller are also on chip.

SMM, the differences provide some power-saving alternatives.

Implementing Intel's SMM also requires its companion, the 82360SL peripheral I/O chip. The chip has a host of on-chip peripherals that are common to an ISA bus computer design, such as DMA, communication, interrupt controllers, and timer counters. The chip generates the SMI to the CPU in response to external system events.

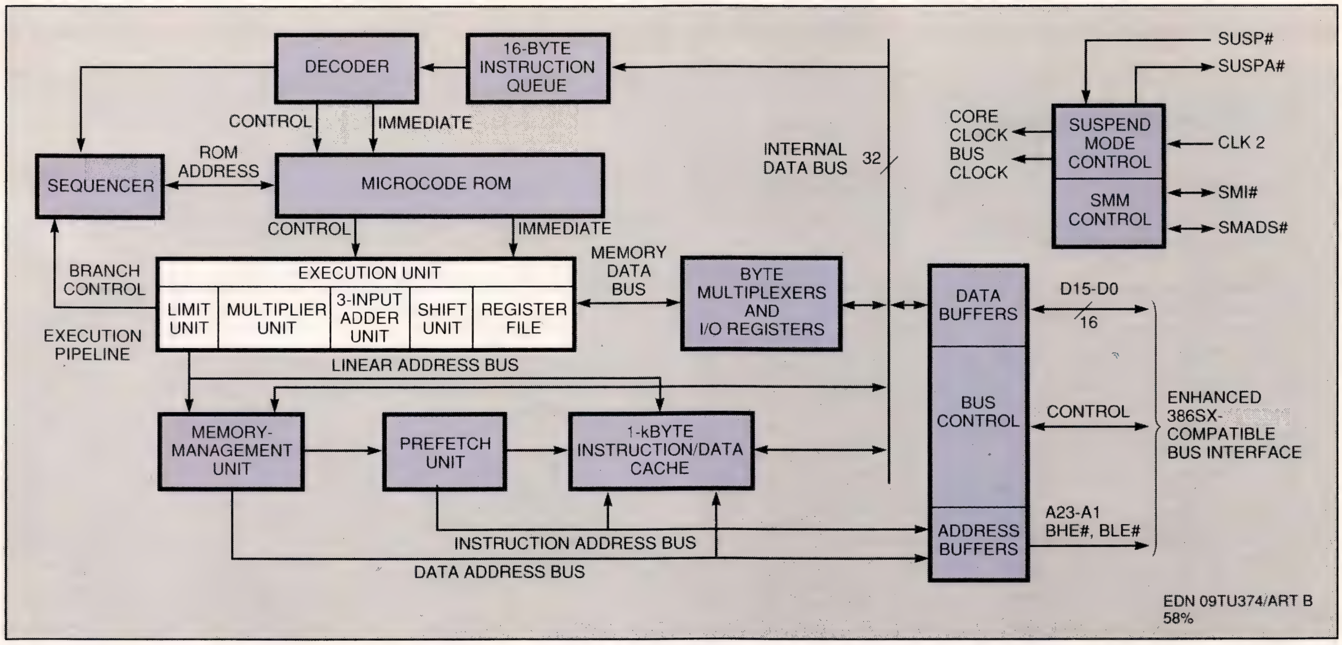
Similar to the i486-based architecture, both i486 SL and Cx486SLC/e μPs have the same general-purpose, segment, instruction, and flag-pointer registers. The chips also have registers that let you access additional features. In the i486 SL μP you access these registers by enabling one of six different configuration spaces. Each configuration space is protected from accidental or unauthorized writes because each access can only occur when the configuration space is enabled.

You can enable a configuration space by writing a bit to a CPUPWR-MODE register, which in turn makes a host of configuration registers visible for the selected space. Because the configuration registers for Intel's SMM reside in the 82360SL chip, you must use this chip to implement SMM. Once the 82360SL configuration space is enabled, you write bits to the SM-REQ-CNTRL register using an index to initialize SMM or 00H to disable SMM features. Clock control registers let you control the speed or stop the clock to the CPU, DMA controller, keyboard controller, and math coprocessor depending on the power-management state.

SMM provides three power-management states: local standby, global standby, and suspend. Suspend is the lowest power state, which basically only powers the memory. A software HALT instruction, or the occurrence of an SMI triggered by a system event, enables SMM. When SMM is enabled, the CPU maps a special memory, called system-management RAM (SM-RAM), into the main memory space between 30000H and 3FFFFH. SM-RAM overlays the existing main memory in this region. The CPU saves the current CPU state in SM-RAM starting at 3FFFFH and stops at 3FFA7H after 22 32-bit transfers.

The CPU then executes a user-written SMM handler code located at system address 38000H to implement power management. A resume (RSM) instruction placed at the end of the SMM handler returns the saved CPU state back to the interrupted application program. If there's an I/O instruction to a powered-down device, an I/O trap can initiate an SMI and cause the SMM handler to power-up the peripheral. The I/O instruction automatically reexecutes upon RSM-instruction execution.

The Cyrix SMM basically functions the same way, but variations can provide other design alternatives. The CPU has a bidirectional SMI pin and a separate address strobe pin (SMADS) to implement SMM. In addition, two separate pins, called suspend request (SUSP) and suspend acknowledge (SUSPA) can place the CPU into a suspend mode while the CPU is executing application software or SMM handler code. Because the SMM configuration registers are lo-



The Cyrix Cx486SLC/e μP features an i386SX bus-compatible interface, a 5-stage pipeline, and a hardware multiplier. A SUSP pin lets you enter a suspend state without using SMM.

LOW-POWER µPs

cated on the CPU chip, SMM is not tethered to a particular peripheral I/O chip. Third-party core-logic chips, such as Headland's HT25 and VLSI's SCAMP II chip set, generate all of the necessary signals to implement the Cyrix SMM.

When an SMI occurs, the Cyrix CPU saves only a subset of the CPU state to SMM memory, which allows rapid entry and exit into SMM. Cyrix added a number of save and restore instructions, which leave you the option of implementing a complete or partial CPU state store. The SMM memory space can range from 4 kbytes to 16 Mbytes, and the base address is programmable to be a multiple of the memory space size. Execution of a resume instruction returns the CPU to the interrupted application program.

The SUSP and SUSPA pins provide a simple method for placing the CPU in the suspend state without having an SMI issued. Some designers, such as Bob Patti, president of ASIC Design Inc (Chicago, IL), finds managing register bits and flags in Intel's SMM "a software nightmare" and finds the extra two pins on the Cyrix chip an expedient alternative to implement the suspend state. A software HALT instruction can also trigger the suspend state.

The AMD's version of SMM for the Am386DXLV and Am386-SXLV µPs gives you additional options. AMD uses an SMI pin and two additional pins, called SMIADS and SMIRDY, to initiate and terminate bus cycles. When an SMI occurs it takes 61 32-bit transfers to save the entire CPU state into SM-RAM. Both INTR and NMI are disabled upon entry into AMD's SMM, whereas the Intel and Cyrix versions respond to these interrupts when executing SMM handler code.

AMD added a number of move instructions, called UMOVs, that let you move byte, word, or double-word register operands to or from main system memory while executing an SMM routine. In addition, the AMD chips have an I/O instruction break enable (IIBEN) input pin that lets system logic implement an I/O trap when an I/O instruction occurs to a powered-down peripheral.

Assertion of the IIBEN pin causes the CPU to drive the bidirectional SMI pin active and then execute handler code to power-up the peripheral. To reexecute the instruction, the handler code must copy the I/O instruction pointer over a default pointer. Both Headland and VLSI core logic chips have the necessary features to handle AMD's SMM.

Of course, all of these low-power µPs utilize 3V power supplies in one fashion or another. Albeit slower, 3V logic can reap as much as 56% power savings over 5V logic. The Cx486SLC/e comes in 3 or 5V versions. AMD µPs operate on a power supply ranging from 3 to 5.5V. Intel µPs have a voltage-tuned 3V core and a flexible memory bus, PI bus, and ISA bus interface that operates from 3 or 5V.

Flexibility has been a watchword in early 3V designs. Many early designs have been plagued by promised—but still unavailable—3V system components. In fact, some horror stories tell of designers' needing to tweak a power-supply potentiometer to voltage-tune some early 3V components to meet specifications. In addition, some system peripherals on the ISA bus, such as floppy-disk drives, don't employ 3V power supplies. To accommodate these mixed-voltage conditions, designers must use ex-

For more information . . .

For more information on the low-power µPs discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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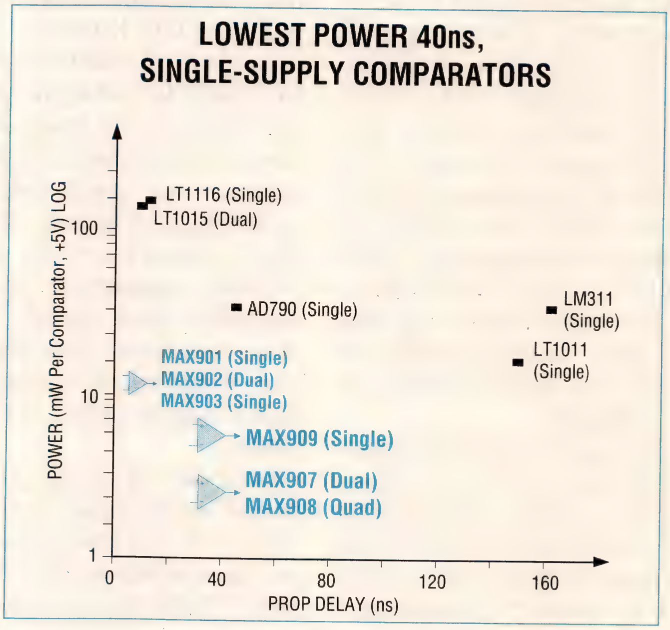

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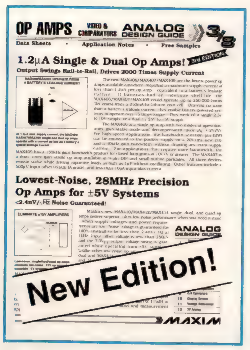

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ternal voltage translators. The problem seems to be dissipating, however, as more 3V components with firm specifications are becoming available in 1993.

Not all designs require the computational power of a 386- or 486-compatible CPU. Many handheld units perform their duties using 8086 code. The 20-oz PC-Lite from Two Technologies (Horsham, PA), and the 2¾-lb Handbook from Gateway 2000 (North Sioux City, SD) use Chips and Technologies' (C&T) F8680 PC/Chip. PC/Chip ($47.50 for 8-MHz 3V version (1000)) runs 8086 opcodes, but a 4-stage pipeline and a 14-MHz clock deliver 80286 performance figures.

To implement power-management techniques, C&T introduced a supervisory mode, called SuperState R. SuperState R has its own hidden memory area, and an event such as an access to an I/O port, an elapsed timer, or an external interrupt can automatically enter the mode. Ill-behaved code in the BIOS or application and terminate-and-stay-resident (TSR) programs cannot disable code written to execute in SuperState R mode.

Instead of slowing or stopping the clock to conserve power, the PC/Chip lets you insert a delay between instructions. SuperState R software can insert delays from 1 to 128 clocks. The delay lets instruction, memory-access, and data-transfer transactions occur at the specified clock speed. The technique eliminates stretching an active state, which is liable to consume power when clocks slow down.

A review of all the µPs for low-power applications is not possible here, but two more processors are worth mentioning. The AT&T Hobbit ATT9200 chip set consists of five devices: the Hobbit µP ($35 (10,000)), system-management controller, PCMCIA (Personal Computer Memory Card International Association) controller, video-display controller, and an optional peripheral controller. The 3.3V chip set runs Go Corp's (Foster City, CA) Penpoint operating system, and EO Inc (Mountain View, CA) employs the chip set in its 440 and 880 personal communicators.

The Hobbit µP employs a 3-stage pipelined RISC architecture that has static branch prediction to minimize pipeline breaks. Instead of general-purpose registers, the µP has a 256-byte stack cache, which eliminates the need to save registers to external memory during procedure calls. The architecture is optimized for running C-language code and features fast interrupt response and context switching. A power-management mode can im-

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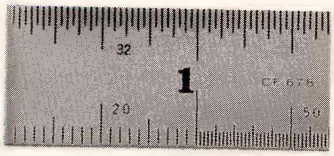

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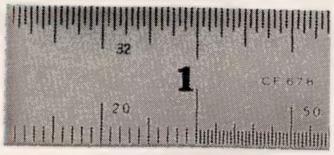

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LOW-POWER μPs

plement four states: full power, idle power, standby, and no power. The mode can also stop any system clock under software control.

Apple Computer chose the ARM (Advanced RISC Machine) 610 μP for the heart of its Newton family of Personal Digital Assistants. Acorn and VLSI Technology codeveloped the ARM family and VLSI distributes it. ARM μPs consist of functional system blocks (FSBs) surrounding a 32-bit ARM 6 RISC core.

The FSBs in the ARM 610 consist of a 4-kbyte instruction and data cache, a write buffer, a memory-management unit, and boundary-scan circuitry. The $46.49 (1000) ARM 610 conserves battery power by having a low-transistor-count design. The chip draws less than 4.5 mA/MHz and operates as fast as 25 MHz.

Not all portable designs require the power of a CISC or RISC μP, however. Mark Freeman, staff engineer at Stratus Inc, a contract house in Seattle, WA, says that a Motorola MCb8HCO5 μC is good enough for most of his portable designs. The chip is resplendent with on-chip peripherals and an instruction set that's adequate for embedded tasks.

The MC68HCO5 has a WAIT instruction that disables CPU processing while the internal clock remains active. A STOP instruction turns off the internal clock. However, the designer must implement power management in external system logic to control power to external peripherals and to manage the system clock rate. High on Freeman's wish list is a μC having an MC68HC05 core and an internal programmable logic block, which could implement these power-saving features. Perhaps one of the μP vendors is listening. EDN

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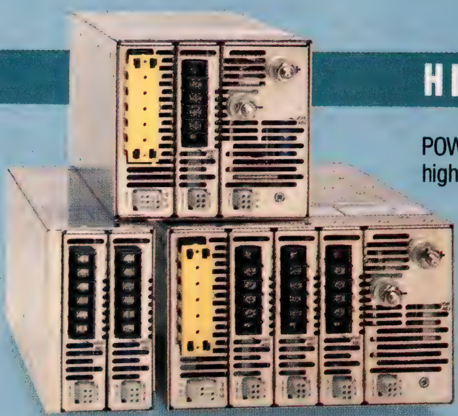

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CIRCLE NO. 49

Two firms reduce the cost of adding color to DSO displays

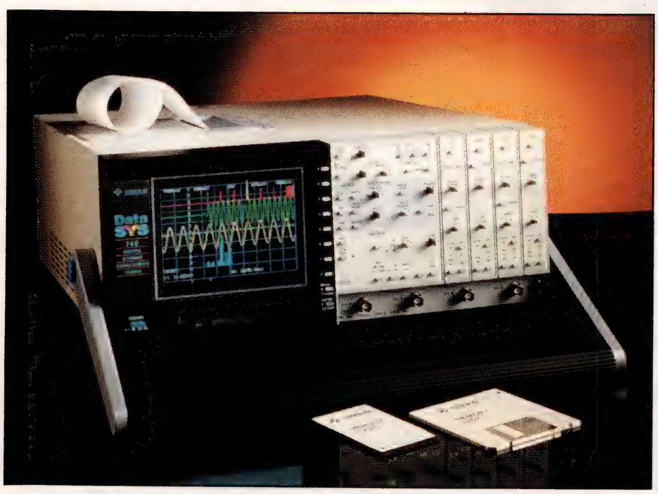
Scopes with color displays offer obvious advantages, but until now, those advantages commanded a high price. When you view several waveforms at once, color makes them easy to tell apart. Depending on how a scope implements color, a multihued display can supply information that is missing from most monochrome DSOs' raster displays, but is inherently present in an analog scope's gray scale. A color scope can also ease the task of telling when two waveforms do and don't coincide. In the past, the problem with color-display scopes was that most were expensive; some cost well over $30,000; others cost close to $60,000. Now however, Gould and Tektronix have altered the cost picture for scopes with color displays.

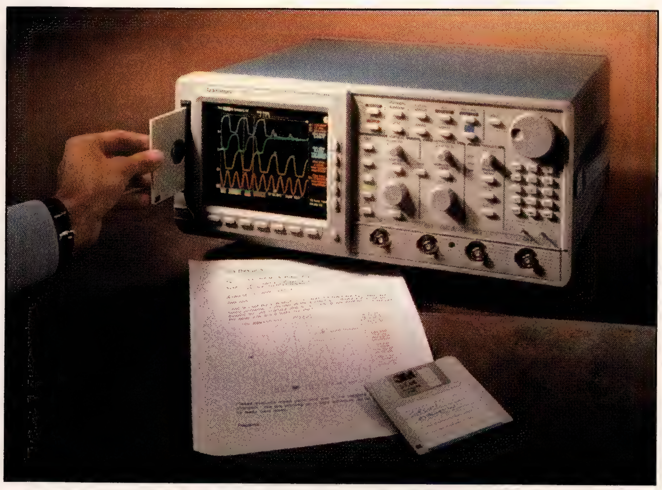
Thanks to new technology, both firms are offering color-display DSOs for about $500 more than the closest equivalent monochrome models. Gould's Datasys 700 series uses an active matrix LCD. You may ask what's new about that; laptop PCs have had active-matrix color displays for at least two years. But the Gould scopes' double-diode-and-reset technology is quite different from that of PCs' thin-film-transistor active-matrix displays. Liquid-crystal technology is also at the heart of the Tek displays. The TDS 544A and 644A do use CRTs, however. The color results from combining a liquid-crystal shutter with a CRT that uses a 180-Hz field-sequential raster scan.

Both techniques produce stunningly bright, clear traces. On a pure pixel-count basis, Tektronix leads Gould by a wide margin. The resolution of the Tek displays is equivalent to the 640×480 pixels of a PC's VGA (video graphics array) adapter. Because the scopes' 7-in. diagonal screens are much smaller than those of most PCs' color monitors, the effect is exceptional. Gould's pixel counts are lower—256×230. But you have to see the Gould display to believe it. Your first impression will be that the 6-in. (diagonal) screen *must* be a CRT. The tiny white text characters are more readable than those on many displays that have 10× as many pixels.

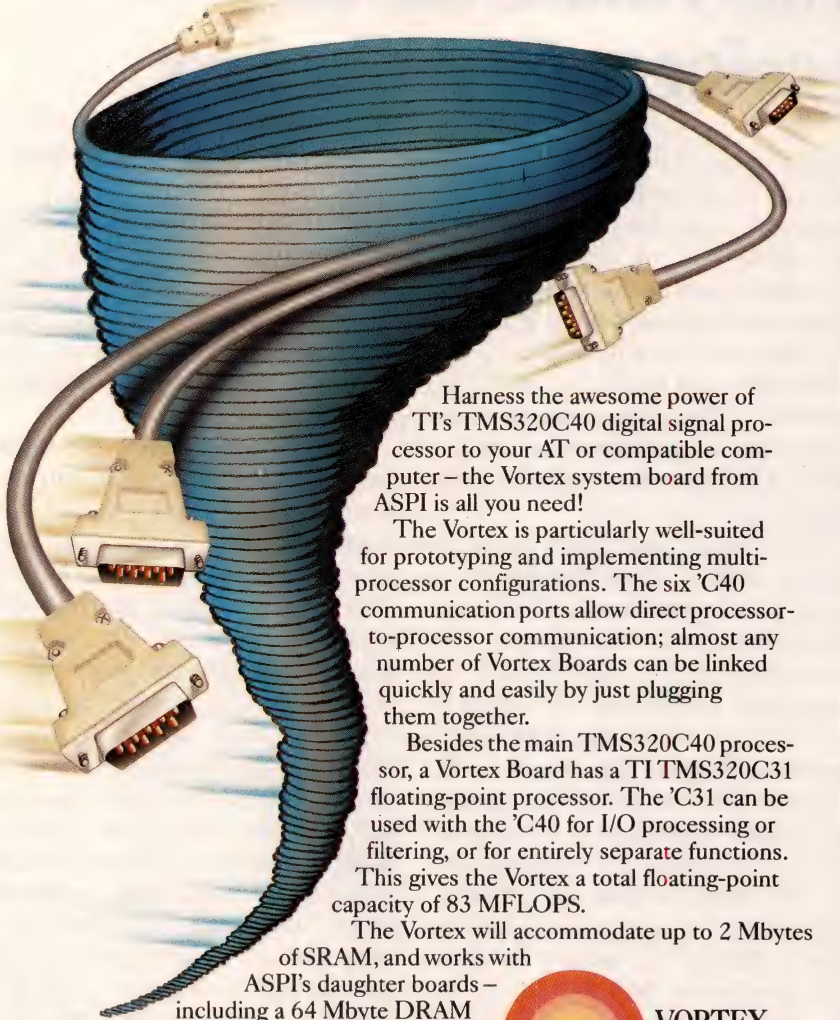
Despite the technological achievements embodied in the displays, the vendors like to mention the color feature almost in passing. What they most want you to hear about are the scopes' other advanced capabilities.

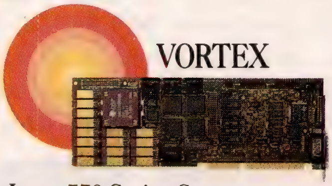
Whereas all of these scopes offer color at a modest premium over monochrome, the Gould and Tektronix units really don't compete. The $7500 Gould unit has 150-MHz bandwidth and can take 100M samples/sec/channel. To make full use of its bandwidth, you must operate it in the random-repetitive sampling mode where it acquires the necessary samples from multiple waveform occurrences. The $16,750 Tek TDS 544A has four 250M-sample/sec ADCs and a bandwidth of 500 MHz. With one channel active, the scope can combine all four ADCs to take 1G samples/sec, just enough to acquire a 500-MHz signal in real time. The $21,490 4-channel TDS 644A always samples in real time. It has a 500-MHz band-





In addition to color, the Gould Datasys 740 (left) offers on-screen readout in user-defined engineering units and a "learn" mode that makes short work of using the front panel to create scope-control programs. The Tektronix TDS 544A (right) and 644A include 3½-in. MS-DOS-compatible floppy-disk drives.





width and can take 2G samples/sec/channel.

The Gould products have several features that are unusual in scopes at the \$7500 price. One is a 50k-sample memory. A zoom capability lets you expand a waveform segment by as much as 1000× and display it beneath the original. The scope also offers a roll (strip-chart) mode that is useful for observing slow phenomena. A host of mathematical operations includes low-pass filtering, "live" multiplication of waveforms, and FFTs. When you work with transducers, the scopes can suppress offsets and scale readings in the engineering units of your choice.

The Tektronix scopes, though similar to the monochrome TDS 540 and 640 that were announced in 1991, incorporate several improvements besides color. One feature not shared by the monochrome units is a 1.44-Mbyte, 3½-in. MS-DOS-compatible floppy-disk drive. Both color scopes also offer a \$1495 video-triggering option that lets them trigger on a variety of currently used video-broadcast formats as well as several proposed HDTV formats. In addition, a FlexFormat capability permits triggering on user-defined HDTV formats and on specific color fields.

The TDS 544A also lets you segment its memory (15,000 points/channel standard; 50,000 optional) and use the different segments to store successive single-shot events at rates to 50,000 events/sec. With a 50,000-point memory, the scope can store 910 waveforms.

—Dan Strassberg

Gould Inc, 8333 Rockside Rd, Valley View, OH 44125. Phone (216) 328-7000. FAX (216) 328-7400. **Circle No. 387**

Tektronix Inc, Box 1520, Pittsfield, MA 01202. Phone (800) 426-2200. **Circle No. 388**

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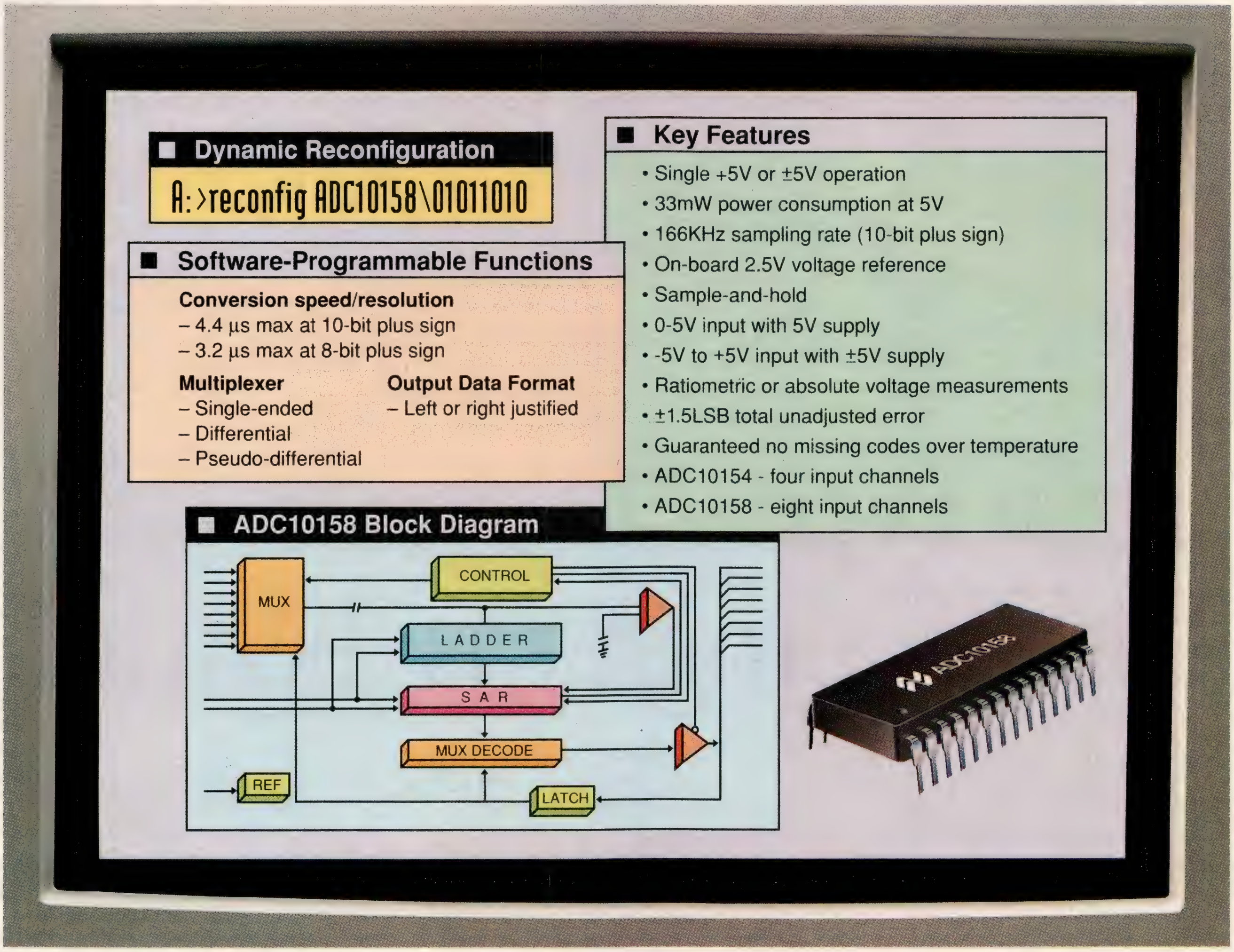

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DATA I/O

CIRCLE NO. 33

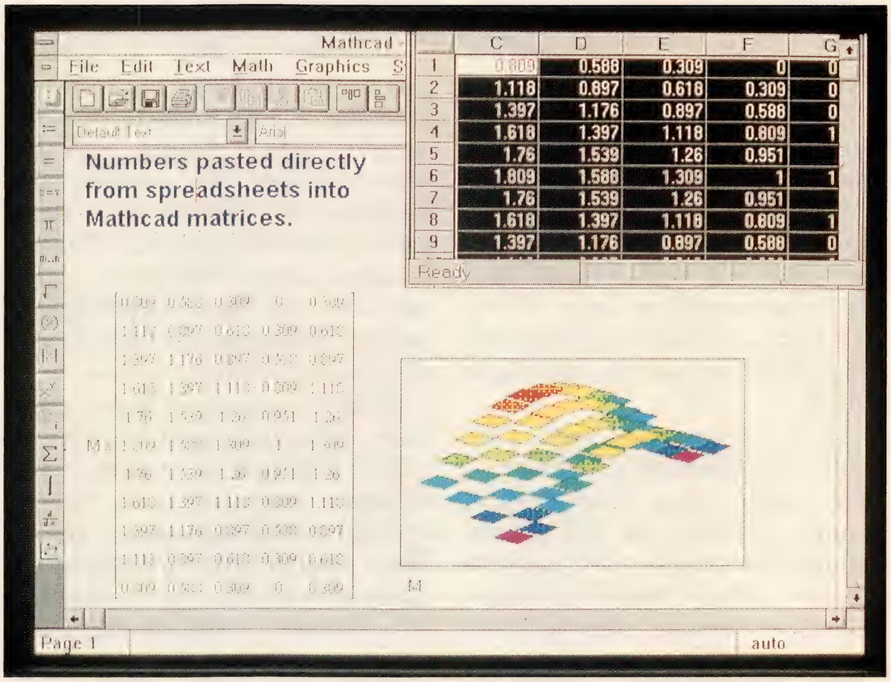
Mathcad 4.0 enhances computations under Windows 3.1

Mathcad 4.0, the latest upgrade to Mathsoft's Mathcad, features a rule-based processor, called Smartmath, which simplifies numeric and symbolic computations. Smartmath reduces symbolic expressions, including integrals and derivatives, before Mathcad computes them. Just like Mathcad's numerical calculations, Smartmath recomputes a symbolic result whenever any of the equations it depends on change.

Mathcad 4.0 runs under Windows 3.1 as a 32-bit application using WIN32S libraries. The software requires a 386- or 486-based PC that runs DOS 3.1 or later and has a minimum of 4 Mbytes of RAM. The company recommends a math coprocessor and 8 Mbytes of virtual memory. Mathcad 4.0 runs twice as fast as previous versions and lets you manipulate virtually unlimited data arrays at one time.

As an alternative to the calculator, Mathcad 4.0 features a toolbar of icons for executing numeric and symbolic calculations; cut-and-paste numbers, which enable you to move data to and from Mathcad to a spreadsheet; and autoscrolling, which lets you scroll through a Mathcad document with a single mouse click. The Auto-equation feature lets you enter equations and text anywhere and then aligns the elements vertically and horizontally; drag and drop lets you highlight part of an equation and move it anywhere. The upgrade also includes extensive new mathematics and graphing features, such as polar and contour plotting, trailing zeros, and *n*th derivative operators.

Mathcad 4.0 supports Microsoft's Object Linking and Embedding (OLE) software for both client and server, which lets you transfer data and graphics between Mathcad and other OLE-compliant software, such as Lotus 1-2-3, Microsoft Word, and Excel. Mathcad 4.0 also provides Dynamic Data Exchange (DDE), which lets other Windows-based applications use Mathcad as a server for complex calculations.



Mathcad 4.0 for Windows 3.1 lets you cut and paste data from a spreadsheet into Mathcad matrices.

Mathsoft also introduced three electronic handbooks, which provide Mathcad 3.1 (or later) users with interactive, accessible technical data. The handbooks are *Theory and Problems of Electric Circuits* from Schaums' Outline Series, Mathsoft's *Topics in Mathcad: Advanced Math*, and *Electrical Engineering*. Schaums' handbook costs $69; the other two handbooks cost $99 (all three require Mathcad 3.1 or later and 1 to 3 Mbytes of hard-disk space).

In addition, five new handbooks for the Mathcad Education Library include *Algebra I*, *Algebra II*, *Pre-calculus*, *Calculus*, and *Differential Equations*. The Educational Library targets students, as well as secondary- and college-level educators. These tools allow users to work with "live" mathematics and explore math concepts without doing routine, repetitive work. The handbooks, which cost $69, require Mathcad 3.1 or later. Mathcad 4.0 requires 4 Mbytes of memory and costs $495 (upgrades cost $49.99).

—John Gallant

Mathsoft Inc, 201 Broadway, Cambridge, MA 02139. Phone (617) 577-1017. FAX (617) 577-8829.

Circle No. 389

14- and 16-bit ADCs speed past the 1-MHz mark

High-speed and high-resolution A/D converters are reaching new performance levels. Analogic Corp introduces a 16- bit, 2-MHz device, and start-up Edge Technology announces a deluge of new products, including a series of 16-bit, 1- to 3-MHz converters and higher-speed 14-bit converters and data-acquisition systems.

Edge Technology's ET1663 is the first 3-MHz, 16-bit ADC. And, along with the specifications listed in **Table 1**, the ET1663 boasts less than 1 LSB of noise. In designing the 2-MHz ADC4344, Analogic doubled the sampling rate of the ADC4322, a 1-MHz predecessor and reduced the package size to a 46-pin hybrid.

All of the converters listed in the **table** are sampling converters—they include either front-end S/H (sample-and-hold) or T/H (track-and-hold) amplifiers. The converters also include precision voltage references, timing circuitry, and some sort of 16-bit quantizer.

The ADC4322 uses a 2-pass, subranging architecture that includes a very stable 16-bit linear reference DAC. This converter's S/H amplifier provides low noise (28 $nV/\sqrt{Hz}$), jitter of 5 psec, and a full-scale step response of 250 nsec for time-domain applications. Noise is typically 90 μV rms for a 10V p-p full-scale range. The part requires ±15 and 5V supplies.

Designers at Edge Technology use monolithic parts and a unique trimming scheme to produce its converters, which require ±15 and ±5V supplies. The company also packages the converters in metal cases, which combined with the converters' power consumption, eliminate the need for an external heat sink and minimizes electrostatic and electromagnetic interference.

All of the converters have a maximum differential nonlinearity of ±0.75 LSB and no missing codes. However, comparing these converters' dynamic specifications is tricky. Even though both manufacturers quote an S/N ratio, each uses different methods to specify distortion. Analogic uses peak distortion, total harmonic distortion (THD), and THD plus noise. These specs are −92 dB max, −86 dB max, and 83 dB min, respectively, for 100-kHz, 0-dB inputs. For the ET1663 family, Edge Technology quotes a spurious-free dynamic range of 92 dB min and SINAD (S/N ratio and distortion) of 83 dB min with 100-kHz, −0.5-dB inputs. The spurious-free dynamic range is typically 100 dB for 5-kHz inputs.

Edge Technology's DAS4504 and DAS4808 are 4-channel, 5-MHz, and 8-channel, 8-MHz data-acquisition systems, respectively. These systems have all the components of the company's 14-bit tracking converters in addition to input multiplexers and buffer amplifiers.

—Anne Watson Swager

Analogic Corp, 360 Audubon Rd, Wakefield, MA. 01880. Phone (508) 977-3000, ext 2089. Fax (617) 245-1274. **Circle No. 385**

Edge Technology, 15 Pine St, Lynnfield, MA 01940. Phone (617) 334-3330. Fax (617) 334-3539. **Circle No. 386**

Table 1—High-speed, 14- and 16-bit sampling ADCs and data-acquisition systems

Vendor	Part no.	Resolution (bits)	Sampling rate (MHz, max)	S/N ratio (dB)	Package type	Power dissipation (typical W)	Price (100)
Analogic Corp	ADC4322	16	2	86 min, 90 typ (100-kHz, 0-dB input)	1.5 × 2.38 × 0.225-in. hybrid	2.6	$995
Edge Technology	ET1663 ET1662 ET1661	16	3 2 1	90 min, 92 typ (100-kHz, −0.5-dB input)	3 × 4 × 0.4-in. module	3.8	$1795 or $1995 $950 or $1295 $499 or $599
	ET1465	14	5	80 min, 82 typ (100-kHz, −0.5-dB input)	3 × 4 × 0.4-in. module	1.8	$495 or $795
	ET1471	14	10	80 min, 82 typ (500-kHz, −0.5-dB input)	3 × 4 × 0.4-in. module	4.2	$1250 or $1495
	DAS4504 DAS4888	14	5 8	80 min, 82 typ (100-kHz, −0.5-dB input)	3 × 4 × 0.4-in. module	2 4.7	$821 or $971 $1688 or $2021

Note: Edge Technology offers two versions of its products; the lower price is for industrial versions.

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CIRCLE NO. 91

Video op-amp prices drop to new depths

Almost unbelievably, you can now buy some video op amps for under $2 in 100-piece quantities. Prices for larger quantities drop much lower. Amplifiers in dual and quad packages, which sometimes have less impressive specs than the single versions, are as low as $1.12 per amp.

The products in **Table 1** join high-speed amplifiers from Analog Devices, Elantec, and Linear Technology, as well as from Burr-Brown, Comlinear, Harris Semiconductor, Maxim Integrated Products, National Semiconductor, and SGS-Thomson. The competition between these vendors seems most intense with current-feedback devices, but many high-speed amplifiers use the voltage-feedback topology.

In addition to 3-dB bandwidth, other specifications that differentiate high-speed amplifiers—especially those tailored for video applications—are output current, differential gain and phase, and gain flatness.

The LT1252 current-feedback op amp features differential gain of 0.01% and phase of 0.09°. The dual and quad versions feature 0.03% and 0.28° differential gain and phase, respectively. The AD818 voltage-feedback device features 0.05° and 0.01% differential phase and gain. Differential gain and phase for the EL2x44 family are 0.04% and 0.15°, respectively. The EL2x60 devices specifications are 0.04% and 0.1°.

For a video amplifier, 100 mA is a high output drive. The EL2x60 has a minimum and typical output current of 60 and 100 mA, respectively. The LT1252 has a minimum output current of 30 mA; the AD818, 50 mA; and the EL2044 minimum is 50 mA. The 0.1-dB bandwidth of the AD818 is 55 MHz, compared to the LT1252's 30 MHz.—**Anne Watson Swager**

Analog Devices Inc, 181 Ballardvale St, Wilmington, MA, 01887. Phone (617) 937-1428. Fax (617) 821-4273. **Circle No. 382**

Elantec, 1996 Tarob Ct, Milpitas, CA, 95035. Phone (408) 945-1323. Fax (408) 945-9305. **Circle No. 383**

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA, 95035. Phone (408) 432-1900. Fax (408) 434-0507. **Circle No. 384**

Table 1—Recently introduced low-cost, high-speed op amps

Vendor	Part no.	Characteristics	Price (100)
Analog Devices Circle No. 382	AD818	100-MHz bandwidth at gain of −1. 50-mA output current. 7.5-mA supply current. (Higher-speed version of company's '817.)	$1.99
	AD826/828	Dual versions of '817 and '818.	$2.99/$3.99
Elantec Circle No. 383	EL2044/2244/2444	Singles, duals, and quads at 60-MHz, unity-gain-stable bandwidth. 5.2-mA supply current.	$1.80/$2.95/$3.95
	EL2260/2460	Dual and quad 100-MHz bandwidth.	$5.20/$8.40
Linear Technology Circle No. 384	LT1252/3/4	90- to 100-MHz bandwidth. 0.1-dB flatness to 30 MHz.	$1.75/$2.49/$4.49

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MobilExpo '93

Tentative Site Itinerary
May 10 to June 23 (2nd Half)

ATE	TIME	LOCATION
/10 londay	9:00-11:00 AM	RAYTHEON ELECTRO-MAGNETIC SYSTEMS 6380 Hollister Avenue, Goleta, CA
/10 londay	12:00-3:00 PM	DELCO SYSTEMS OPERATIONS 6767 Hollister Avenue, Goleta, CA
/11 uesday	8:30-10:30 AM	HUGHES MISSILE SYSTEMS COMPANY 8433 Fallbrook Avenue, Canoga Park, CA
/11 uesday	11:30-1:30 AM-PM	LITTON GUIDANCE & CONTROL SYSTEMS 5500 Canoga Avenue, Woodland Hills, CA
/12 /ednesday	9:30-1:00 AM-PM	JET PROPULSION LABORATORIES 4800 Oak Grove Drive, Pasadena, CA
/12 /ednesday	2:15-4:15 PM	LORAL LIBRASCOPE CORPORATION 833 Sonora Avenue, Glendale, CA
/13 hursday	10:00-2:00 AM-PM	LAWRENCE LIVERMORE LABORATORIES 7000 East Avenue, Livermore, CA
/14 riday	8:30-10:30 AM	WATKINS-JOHNSON COMPANY 3333 Hillview Avenue, Palo Alto, CA
/14 riday	11:30-2:30 AM-PM	LOCKHEED MISSILES & SPACE COMPANY 1111 Lockheed Way, Sunnyvale, CA
17 onday	9:00-11:30 AM	SUN MICROSYSTEMS, INC. 2550 Garcia Avenue, Mountain View, CA
17 onday	1:00-4:00 PM	SILICON GRAPHICS 2011 N. Shoreline Blvd., Mountain View, CA
18 uesday	8:30-11:00 AM	APPLE COMPUTER, INC. 20650 Valley Green, Cupertino, CA
18 uesday	1:00-3:30 PM	APPLIED SIGNAL TECHNOLOGY 160 Sobrante Way, Sunnyvale, CA
19 ednesday	8:30-11:00 AM	3COM CORPORATION 5400 Bayfront Plaza, Santa Clara, CA
19 ednesday	11:45-1:30 AM-PM	STANFORD TELECOM, INC. 2421 Mission College Blvd., Santa Clara, CA
19 ednesday	2:15-4:15 PM	SCHLUMBERGER TECHNOLOGIES 1601 Technology Drive, San Jose, CA
20 ursday	8:30-10:00 AM	WATKINS-JOHNSON COMPANY 2525 North First Street, San Jose, CA
20 ursday	11:00-1:00 AM-PM	LORAL WESTERN DEVELOPMENT LABS 3200 Zanker Road, San Jose, CA
20 ursday	2:00-4:00 PM	CONNER PERIPHERALS INC. 3061 Zanker Road, San Jose, CA
21 day	9:30-12:00 AM	UNISYS CORPORATION 2700 North First Street, San Jose, CA
24 onday	9:00-12:00 AM	BOEING COMMERCIAL AIRPLANE (Main Campus) 3003 West Casino Road, Everett, WA
24 onday	1:00-4:00 PM	BOEING COMMERCIAL AIRPLANE (Everett Mall) 906-1010 S.E. Everett Mall Way, Everett, WA
25 esday	10:00-2:00 AM-PM	BOEING MILITARY AIRPLANE CO. 9725 East Marginal Way, Seattle, WA
26 ednesday	8:00-12:00 AM	BOEING KENT SPACE CENTER South 212th Street, Kent, WA
26 ednesday	1:30-4:00 PM	BOEING KENT SPACE CENTER EAST 68th Avenue So., Kent, WA
27 ursday	8:30-11:00 AM	BOEING COMMERCIAL AIRPLANE 8th & Park Streets, Renton, WA
7 ursday	12:00-2:30 PM	SUNDSTRAND DATA CONTROL 15001 N.E. 36th Street, Redmond, WA
8 day	8:30-10:30 AM	INTEL CORPORATION (Hawthorne Farms) 5200 Elam Young Pkwy., Hillsboro, OR
8 day	11:30-1:30 AM-PM	INTEL CORPORATION (Cornell Oaks) 15201 N.W. Greenbrier Pkwy., Beaverton, OR

DATE	TIME	LOCATION
5/28 Friday	2:30-4:00 PM	INTEL CORPORATION (Jones Farm) 2111 N.W. 25th Ave., Hillsboro, OR
6/1 Tuesday	9:30-12:00 AM	PARAMAX CORPORATION, A UNISYS COMPANY 640 North 2200 West, Salt Lake City, UT
6/1 Tuesday	1:00-3:00 PM	E-SYSTEMS INC., Montek Div. 2268 South 3270 West, Salt Lake City, UT
6/3 Thursday	9:00-12:00 AM	STORAGE TECHNOLOGY CORPORATION 2345 Clover Basin Dr., Longmont, CO
6/3 Thursday	1:00-4:00 PM	STORAGE TECHNOLOGY CORPORATION 2270 South 88th Street, Louisville, CO
6/4 Friday	8:30-11:00 AM	AT&T BELL LABORATORIES 11900 N. Pecos Street, Denver, CO
6/4 Friday	12:00-3:00 PM	MARTIN MARIETTA CORPORATION 12257 Colo. State Hwy. 121, Littleton, CO
6/7 Monday	9:00-11:30 AM	DIGITAL EQUIPMENT CORPORATION 301 Rockrimmon Blvd. S., Colorado Springs, CO
6/8 Tuesday	12:00-3:00 PM	BOEING COMMERCIAL AIRPLANE CO. 3801 So. Oliver, Wichita, KS
6/9 Wednesday	9:00-11:30 AM	ALLIED SIGNAL AEROSPACE, BENDIX/KING 400 North Rogers Road, Olathe, KS
6/9 Wednesday	1:00-3:00 PM	WILCOX ELECTRIC 2001 N.E. 46th Street, Kansas City, MO
6/10 Thursday	9:00-12:00 AM	ALLIED SIGNAL AEROSPACE 2000 East 95th Street, Kansas City, MO
6/11 Friday	9:00-12:00 AM	McDONNELL DOUGLAS CORPORATION Lindbergh & McDonnel Blvd., St. Louis, MO
6/14 Monday	9:00-12:00 AM	ROCKWELL INTERNATIONAL, COMML' AVIONICS 400 Collins Road N.E., Cedar Rapids, IA
6/14 Monday	1:00-2:30 PM	ROCKWELL INTL', COLLINS DEFENSE 855 5th Street N.E., Cedar Rapids, IA
6/15 Tuesday	9:00-1:00 AM-PM	IBM CORPORATION Hwy 52 & Northwest 37th St., Rochester, MN
6/16 Wednesday	10:00-12:30 AM-PM	HONEYWELL INC., MILITARY AVIONICS 1625 Zarthan Avenue, St. Louis Park, MN
6/16 Wednesday	1:30-3:30 PM	HONEYWELL INC., COMML' FLIGHT SYSTEMS 8840 Evergreen Blvd., Coon Rapids, MN
6/17 Thursday	8:30-10:00 AM	ADC TELECOMMUNICATIONS 5900 Clearwater Ave., Minnetonka, MN
6/17 Thursday	10:30-12:00 AM	ADC TELECOMMUNICATIONS 11311 K-Tel Dr., Minnetonka, MN
6/17 Thursday	1:00-3:00 PM	PARAMAX SYSTEMS, A UNISYS COMPANY 3333 Pilot Knob Road, Eagan, MN
6/18 Friday	9:00-11:00 AM	JOHNSON CONTROLS, INC. 507 E. Michigan Ave., Milwaukee, WI
6/18 Friday	12:00-2:00 PM	ALLEN-BRADLEY COMPANY 1201 South 2nd Street, Milwaukee, WI
6/21 Monday	10:00-1:00 AM-PM	SUNDSTRAND ADVANCED TECHNOLOGY 4747 Harrison Avenue, Rockford, IL
6/22 Tuesday	9:00-11:00 AM	HONEYWELL INC. 1500 W. Dundee Road, Arlington Heights, IL
6/22 Tuesday	12:00-2:30 PM	MOTOROLA RADIO-TELEPHONE SYSTEMS 1421 W. Shure Drive, Arlington Heights, IL
6/23 Wednesday	9:30-12:00 AM	AT&T BELL LABORATORIES (Indian Hill Main) 2000 N. Naperville Rd., Naperville, IL
6/23 Wednesday	1:00-3:00 PM	AT&T/NCR CORPORATION (Indian Hill West) 1100 E. Warrenville Rd., Naperville, IL

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CIRCLE NO. 90

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CIRCLE NO. 110

Motorola's 68360 communications controller moves to 32 bits

There are two ways to do higher-bandwidth communications processing: go to a faster CPU or use built-in hardware to handle specialized protocol processing. Motorola took the second route with its 68302, combining a 68K CPU with dedicated communications hardware, including a microprogrammed line processor. Now, to meet rising bandwidth needs, the company has extended the 302 architecture to a full 32 bits of processing (a more powerful CPU). Running with a 25-MHz clock, the 68360 Quad Integrated Communications Controller (QUICC) can run four channels and/or protocols concurrently, with data rates up to 2.048 Mbps/channel.

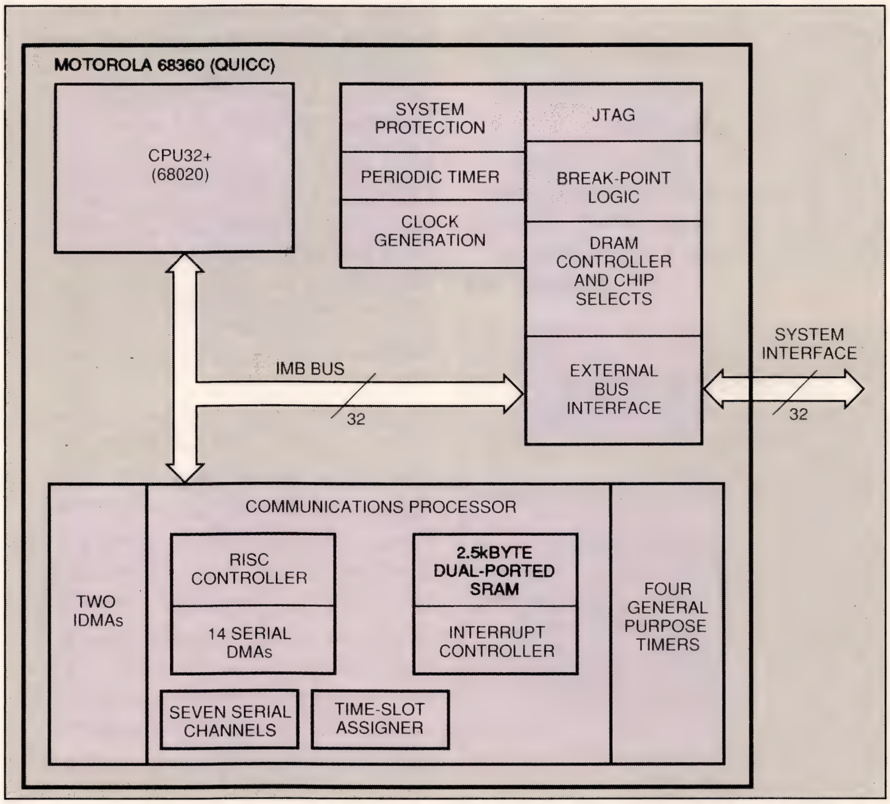
Instead of the 68302's 68000 16-/32-bit CPU, the 68360 relies on the CPU32+, a stripped-down 68020 (less MMU and cache-management instructions). At 25 MHz, the CPU delivers approximately 4.5 native MIPS peak. The company sped up internal operations with a 32-bit, on-chip intermodule bus. This bus, a variation of the 683xx family bus, serves as the on-chip system bus, as well as a mechanism for integrating new modules onto the chip.

The 68360 uses the same basic microprogrammed communications processor as the 68302 to process data on to and off of the serial I/O lines. And, like the 68302, the 68360 relies on dual-ported RAM to move data between the CPU32+ and the communications controller. However, the 68360's static RAM (SRAM) is 2.5 kbytes, compared with the 68302's 1152 bytes.

The 68360 also features four SCCs (serial communication channels), each of which can automatically handle (with the communications processor) eight standard communications protocols. Additionally, the µP has four general-purpose, 16-bit timers (you can cascade two to a 32-bit timer), two IDMA (independent DMA) channels for high speed, 32-bit data transfers, buffer chaining, and independent request/acknowledge logic.

Each SCC can handle multiple protocols through a combination of dedicated hardware and microprogram support. The built-in communications protocols are HDLC/SDLC, HDLC bus, UART, BiSynch, Signaling System 7, LocalTalk, Transparent Mode, and Ethernet (68EN360 on the first serial channel). Communications hardware includes two serial management controllers (SMC), a SPI (serial peripheral interface), and an optional parallel port. Also, a dedicated Time-Slot Assigner (TSA) integrates the serial channels to the single Time-Domain Multiplexed (TDM) bus. The TSA makes it easy to implement TDM interfaces to T1, CEPT, IDL, GCI, ISDN, or Primary Rate protocols. The TSA multiplexes a channel into or from each time division slot. It handles two TDM lines simultaneously.

Also, for the first time, Ethernet is built into a 683xx communications controller. The 68EN360, a version due in September, implements the Ethernet MAC (media access) layer in hardware and microcode. Thus, with this controller on your mother board, you can easily build a bridge



Built around a 68020, the 68360 can simultaneously process four complex communications protocols. It features dedicated communications hardware, including a microprogrammed processor.

between a WAN and a local Ethernet LAN on any desktop.

For more processing power, you can run the 68360 slaved to a 68040. In Slave Mode, the 68360's processor is locked up, and the chip functions as a peripheral chip to the external processor. If the processor is sufficient, but you need more channels, you can slave one 68360 to another.

Additionally, the 68360 requires a minimum of support logic. You can just add memory and start the 68360 running. An on-chip memory controller interfaces to SRAM, DRAM, Flash, and EEPROM. The 68360 handles up to eight memory banks, with up to 15 programmable wait states.

For evaluation and debugging code, Motorola supplies a QUICC Application Development System (QUADS), which includes a board with a 68360 for evaluation. You can also use it as a low-cost ICE by plugging it into a target board and relying on the 68360's background debug mode for control. QUADS costs $1995.—**Ray Weiss**

Motorola Inc, Microprocessor and Memory Technologies Group, 6501 William Canon Dr W, Austin, TX 78735. Phone (512) 891-2000.

Circle No. 393

Motorola 683xx communications controller

- 25-MHz clock
- CPU32+ (68020 core)
- Microprogrammed communication CPU
- 2.5-kbyte dual-ported SRAM
- 32-bit IMB internal-chip bus
- Glueless memory interface, memory controller—SRAM, DRAM, EEPROM
- External bus: dynamic sizing (8, 16, 32 bits); 28- to 32-bit address
- On-chip hardware breakpoints
- 4 SCCs
- 7 external interrupts
- 240-lead PQFP, PGA
- $49.90 (10,000) sample qty
- Ethernet, $59.90 (10,000)

24-bit DSP chip drops power to 165 mW at 40 MHz

Many designers equate DSP chips with high-throughput, math-oriented processing, but not low-power operation. Not true. As DSP μPs move into mainstream embedded processing, they're taking on many properties of the microcontrollers they're competing with. Motorola's 24-bit 56002 DSP family is easing down the power-dissipation curve: The 3V DSP56L002 dissipates 165 mW (typ) while running at 40 MHz.

The DSP56002/1 24-bit processor family fills the gap between low-end 16-bit DSP chips and the faster, more expensive 32-bit DSP μPs. Twenty-four bits provide a large data word for digital audio, telecommunications, and consumer applications. Like most DSP chips, the 56002/1 is pipelined and delivers apparent single-cycle execution for most instructions. Its peak performance approaches 25 native MIPS.

Motorola DSP56L002 24-bit DSP μP

- 40-MHz clock (static); programmable PLL, 10 kHz to 40 MHz
- 24-bit ALU fed by internal data paths; 2 56-bit accumulators
- 3-stage pipeline, 50-nsec/stage
- 3 data RAMs (256, 256, and 512 24-bit words)
- 2 256-word, 24-bit program ROMs
- External bus: 24-bit addr, 16-bit data
- On-chip emulation-support circuitry
- 3 external interrupts
- 3.3V, 165 mW (typ)
- $47 (1000) in 132-pin plastic QFP

The low-power DSP56L002 is fully pin and instruction compatible with earlier 56001/2 DSP chips. Motorola engineers reworked the chip only to reduce power. The new chip is fully static and entirely CMOS, unlike earlier family members. In addition, peripherals—including memories—that the chip does not use or address are switched off to save additional power.

Because the DSP56L002 is a static chip, you can put it to sleep and then stop the clock entirely to really cut power. The on-chip PLL lets you adjust the clock rate to run no faster than needed for a given application. The PLL's 12-bit divider lets you select a clock rate from 10 kHz to 40 MHz.

A classic DSP architecture, the DSP56L002 has automatic hardware loop control, two data-address generators, and multiple internal address and data buses for high-speed, parallel operations. The external interface comprises a 16-bit data bus and 24-bit address bus. The three separate address spaces (X data, Y data, and P program) let you fetch the next instruction, retrieve the next X and Y parameters, and execute the instruction all within the 3-stage pipeline.

—**Ray Weiss**

Motorola Inc, Microprocessor and Memory Technologies Group, 6501 William Cannon Dr W, Austin, TX 78735. Phone (512) 891-2030. Fax (512) 891-3874.

Circle No. 396

TMS370C 8-bit μC moves up to 32 kbytes of ROM/EPROM

Today's 8-bit μCs can take on more and more work. Yesteryear's 4- and 8-kbyte memory sizes are no longer large enough for today's more complex applications. Now, TI's TMS370C series 8-bit μCs can handle applications that need up to 32 kbytes of on-chip program memory.

The TMS370 family of 8-bit μCs

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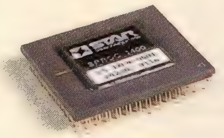

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Adaptive noise canceler	DSP	6 months	**1 week**	**$57,500***
Power supply controller	analog	6 months	**1 day**	**$60,000***
Closed-loop vibration controller	analog	3 months	**2 weeks**	**$240,000†**

†Total system savings including project overhead, engineering resource, and system hardware costs.
*Estimated savings in engineering resource based on cost of $10,000 per man month.

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The Signal Processing Company

CIRCLE NO. 65

EDN MAGAZINE AND EDN PRODUCTS & CAREERS INNOVATION '92

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50MHz SPROC Now Available!

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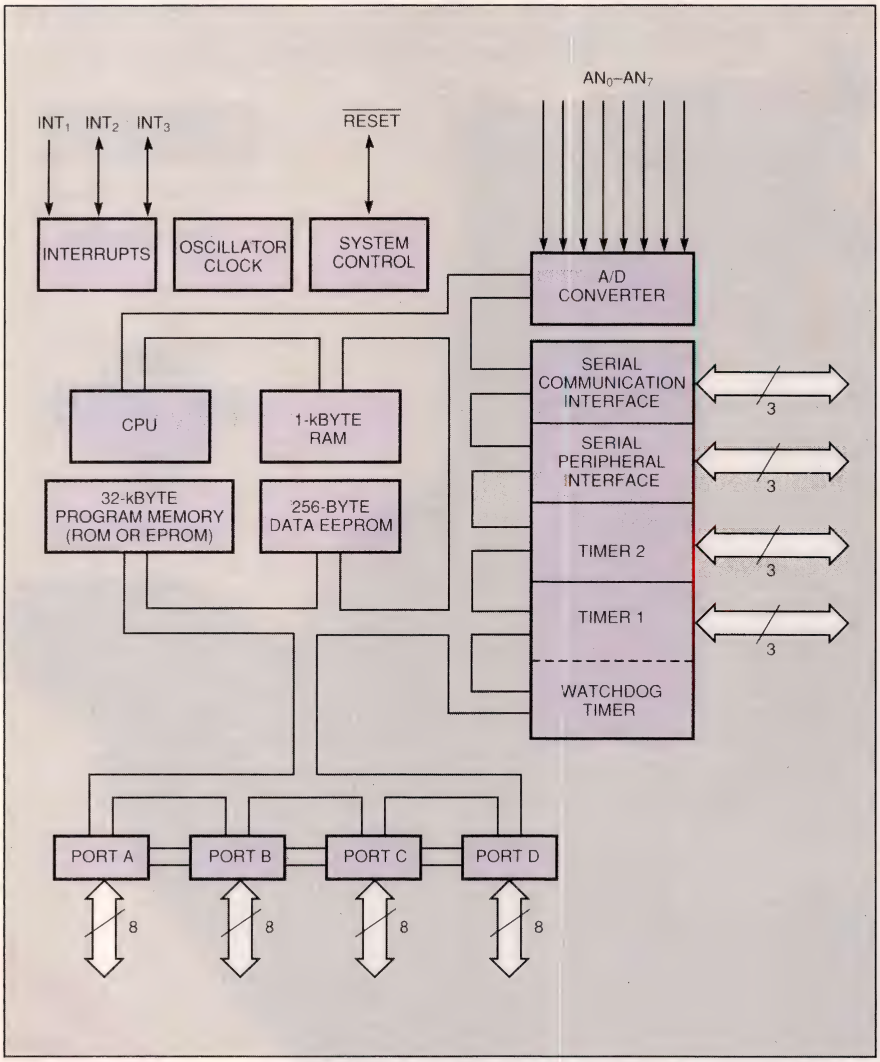
is designed for low-end and automotive applications. The TMS370Cx58 controller combines 32 kbytes of ROM/EPROM with 1 kbyte of static RAM (SRAM) and 256 bytes of EEPROM.

The TMS370 8-bit µC family has a surprisingly full set of peripherals, including an A/D converter, a watchdog timer, a serial communications interface (SCI), a serial peripheral interface (SPI), and complex timers.—**Ray Weiss**

Texas Instruments Inc, Semiconductor Group, Box 809066, Dallas, TX 75380. Phone (800) 336-5236, ext 3990. **Circle No. 397**

TMS370Cx58 8-bit µC
- 2- to 20-MHz clock (internal div-by-4)
- 256 registers in RAM
- 32-kbyte ROM/EPROM, 1-kbyte SRAM
- 256-byte data EEPROM
- 55 I/O pins
- 24-bit watchdog timer
- 2 16-bit timers with 4 compare registers or PWM outputs
- 8-channel, 8-bit ADC
- SCI, SPI
- 3 external interrupts
- In 68-lead PLCC, $10 (25,000 qty/year)



The Texas Instruments' TMS370 8-bit µC has a register-oriented architecture with 256 registers held in RAM. The µC handles register-to-register operations and has 14 addressing options.

Drive an 8-bit PIC µC with Basic

If you're performing simple control functions, you don't have to use the hard-to-maintain assembly language to run µC applications. Believe it or not, many engineers use Basic to drive 8051s and 68HC11s, and also the low-cost Microchip Technologies' PIC µC. Now from Parallax comes Basic Stamp—a packaged Basic development and prototyping system that includes the PIC µC with Basic in ROM.

The Basic Stamp development package consists of
- Software—a Basic editor, tokenizer, and downloader that run on a PC;
- A 1x2-in. prototyping board—a processor, a 256-kbyte serial EEPROM to hold the Basic tokens, a prototyping area, and a power supply;
- A µC—the 8-bit Basic PIC16C56, running at 4 MHz with the Basic token interpreter in OTP (one-time-programmable) EPROM. Eight I/O pins are available for application I/O.

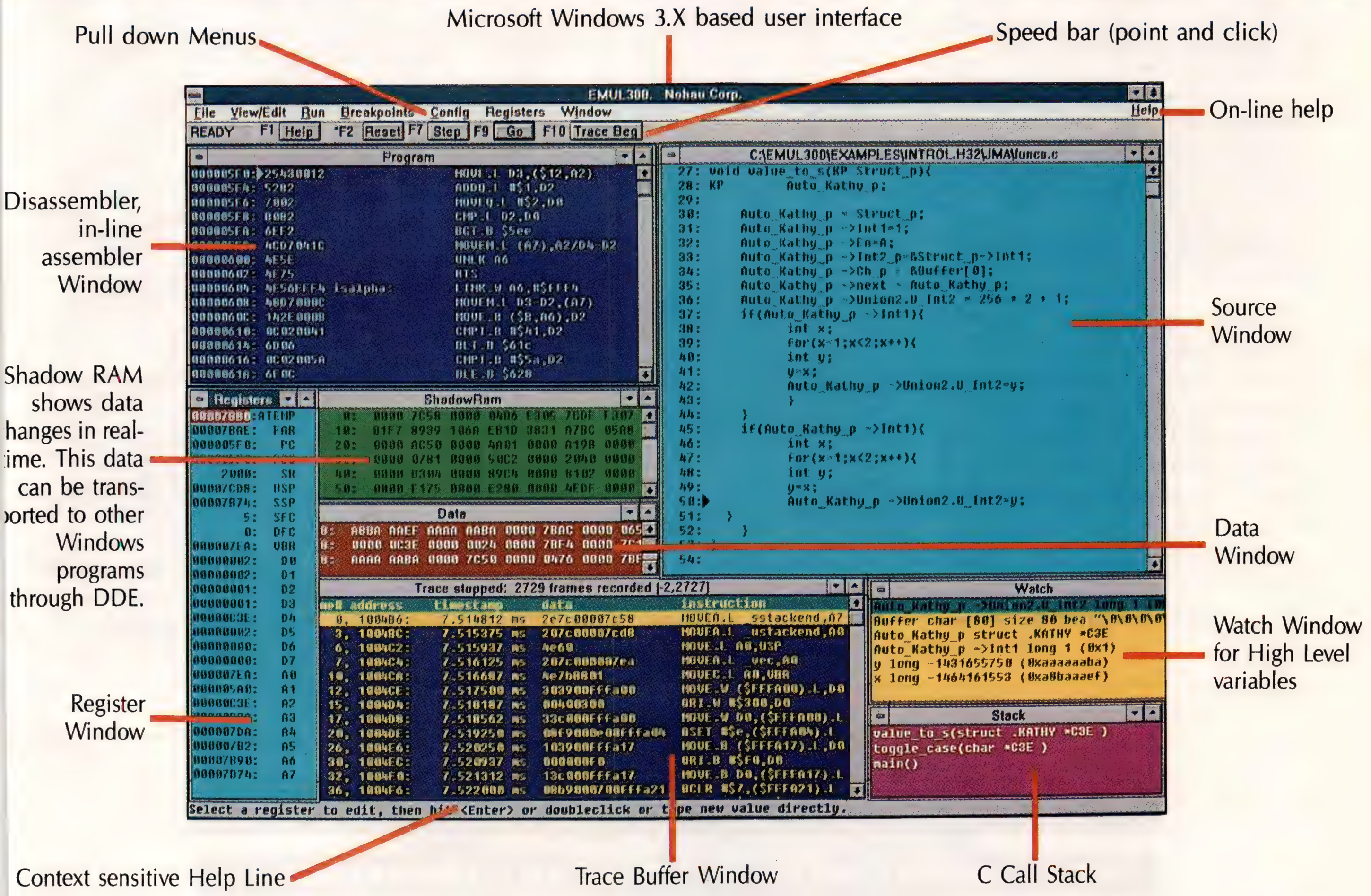
When Parallax designers integrated Basic with the PIC µC, they placed the Basic token interpreter in fixed, on-chip program memory. The development software, however, converts the Basic program into tokens and downloads the program into a serial EEPROM on the Basic Stamp board, rather than placing it in on-chip memory. The CPU executes the program by reading the tokens from the EEPROM.

The serial EEPROM holds roughly 80 to 120 Basic instructions; it can also hold application parameters. The Basic Stamp CPU executes about 2000 Basic instructions per second, which is adequate for a range of low-level applications.

The system uses a subset of Basic that Parallax has extended for real-time control. The operations include

In-Circuit EMULATORS and BACKGROUND Debuggers

68300 68HC16



FEATURES

- Supports both the 683xx and 68HC16 families.
- User Interface under Microsoft Windows.
- Modular approach: From low cost to full feature.
- Real-time emulation at maximum chip speed.
- High-Level C support with in-depth support for Intermetrics, Introl, Microtec, Sierra and more. In-line assembler and disassembler.
- Hardware and software breakpoints.
- Up to 4 Mbytes of emulation RAM
- Trace board, up to 512k records deep, 104 bits wide, 40 bit timestamp.
- Triggering and filtering, with full pipeline decoding.
- Code Coverage. Program Performance Analysis.
- Memory Contents available in real-time (Shadow RAM).
- DDE support to transfer Shadow Ram to other Windows applications.

8051 68HC11

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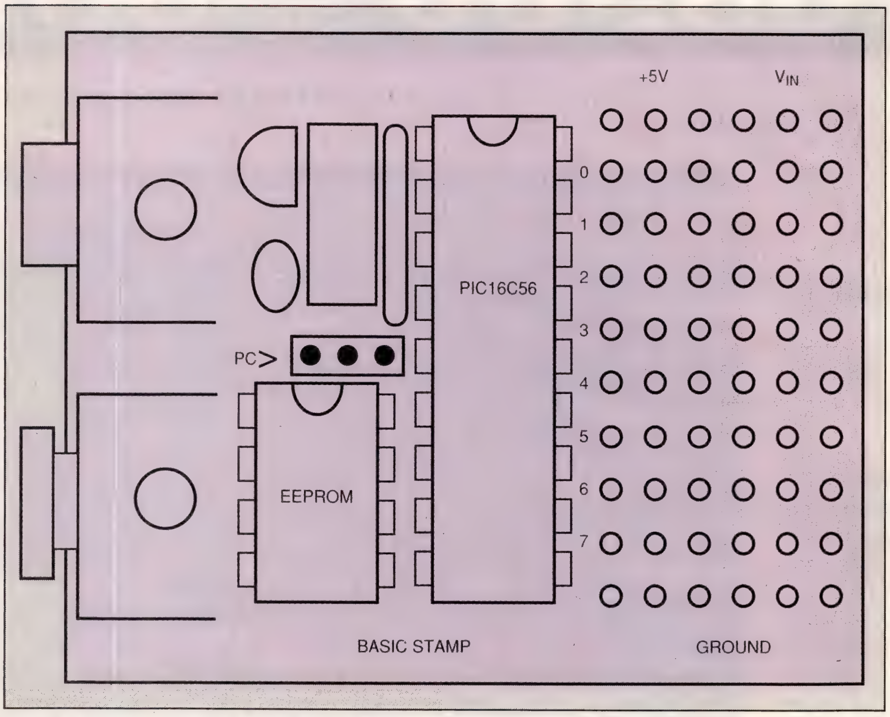
CIRCLE NO. 101

Parallax Basic Stamp (PIC16C56)

- Development package includes software, prototyping board, and PIC16C56 with Basic in ROM. Software runs on IBM PC/XT/AT, DOS 2.0+. $139
- Basic Stamp board includes µC, EEPROM and power supply. Powered by 5 to 12V dc (or 9V battery), 2 mA (typ). $39
- Basic ROMed PIC16C56, $6 (500)

outputting a PWM signal, reading a potentiometer, inputting or outputting a serial I/O data stream, performing digital output or input, reading EEPROM, pausing, controlling power (NAP, SLEEP, END), and sending variables to the PC for debugging. —**Ray Weiss**

Parallax Inc, 6359 Auburn Blvd, Suite C, Citrus Heights, CA 95621. Phone (916) 721-8217. Fax (916) 721-1905. **Circle No. 398**



Using Basic to run an 8-bit PIC µC, you can monitor push buttons, potentiometers, and I/O pins. You can also drive audio, PWM, serial, digital I/O-pin outputs.

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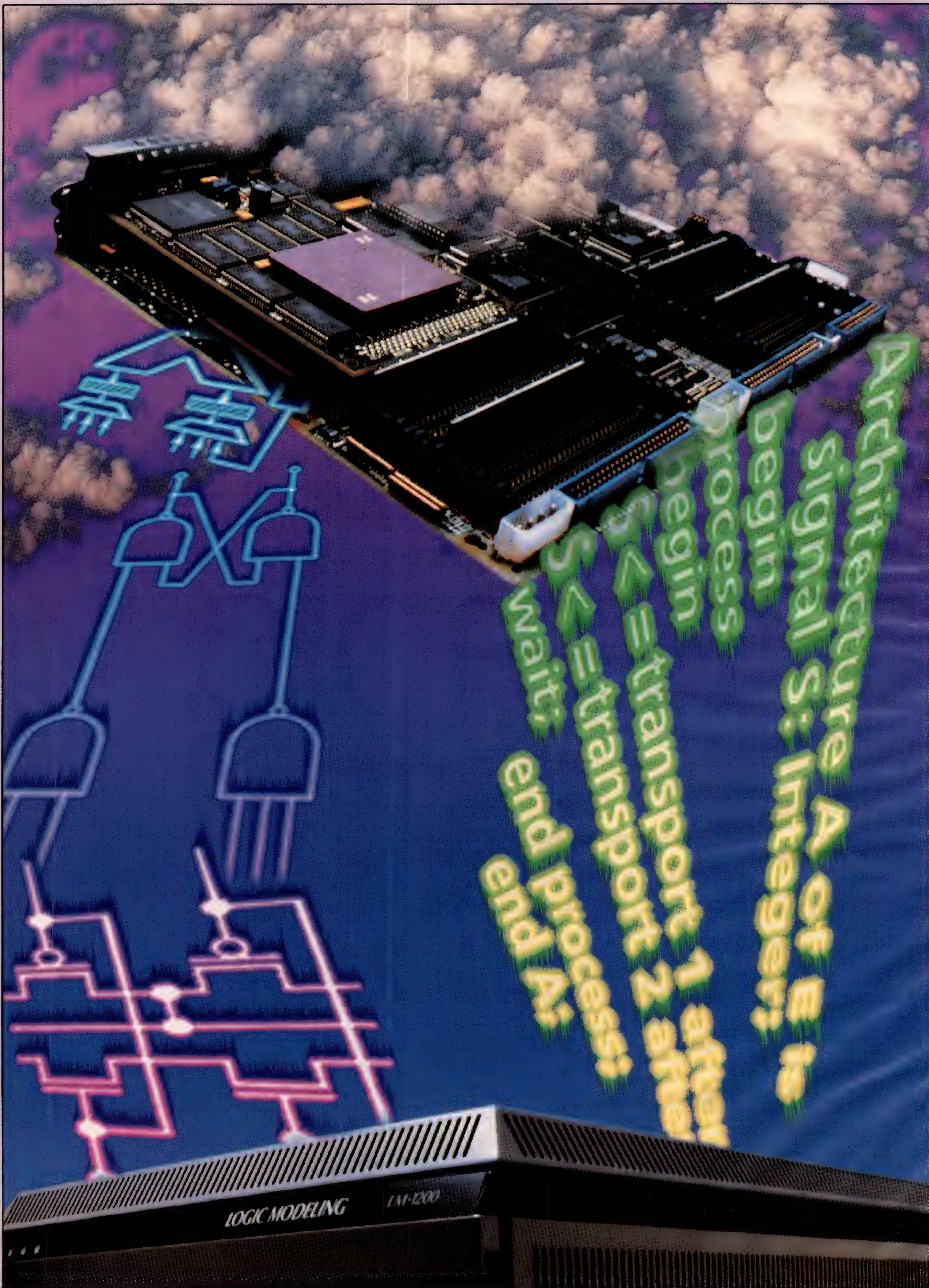

Architecture A of E is
signal S: Integer;
begin
process
begin
S <= transport 1 after
S <= transport 2 after
wait;
end process;
end A;
LOGIC MODELING
LM-1200

Multilevel ASIC modeling

John C Napier, Technical Editor,
with Julie Anne Schofield, Senior Associate Editor

Capitalism collides with engineering when you ask semiconductor vendors for detailed simulation models of complex standard cells or cores. Beyond issues of model accuracy and speed, intellectual-property concerns and the lack of standard model formats will force you to mix gate- and higher-level models to simulate complex ASICs.

You can't put a complex microprocessor on today's typical 20,000-gate ASIC. But as gate counts rise into the hundreds of thousands this year, you'll soon be able to use complex LSI (large-scale integration) functions as the core of your designs.

Like most ASIC designers, you probably rely on gate-level design and simulation to verify functions and timing. But you'll hit a brick wall when you ask for gate-level models of complex parts. By giving you such a model, a part maker would also be giving you the ability to clone the part (see **box,** "The risks of creating models"). Instead, you'll get a higher-level model, which will eliminate the option of flattening your whole design to the gate level for simulation.

Microprocessor vendors don't want to give away the store, so you'll have to mix their high-level models with gate-level models to simulate complex ASICs. (Photo courtesy Logic Modeling Inc)

Unfortunately, there are no standards for passing timing and function information between gate- and higher-level models (see **box,** "VITAL team pursues VHDL timing standards"). Until standards emerge, you'll have these options for modeling complex ASICs: You can use the available high-level models; you can use a hardware modeler to connect existing ICs to a simulation of your new peripheral and application-specific circuitry; or you can reuse your own designs as cores.

Hardware description languages such as VHDL (VHSIC HDL) and Verilog serve as the most common vehicles for describing and modeling multilevel designs. One common approach for using the available models is to run nonsynthesizable behavioral VHDL models with gate-synthesizable peripheral models. You link the binary files supplied by the part maker with your design's binary files compiled from your source code.

Part makers block the use of logic synthesis as a reverse-engineering tool by distributing only object code and bus-functional behavioral models. Bus-functional models mimic only bus activity (read-write cycles) for a processor, and so run faster than behavioral models that handle all instructions and processor I/O. (It's rare to find a full-function model for complex microprocessors because the work involved in writing such a model is comparable to that of designing the

The risks of creating models

No matter who employs them, model writers generally don't get access to information that could let others reverse-engineer the chip. In an ideal world, the chip designer would write the model. In practice, several layers of information laundering separate the model writer from the hardware design team. From the part maker's point of view, a model should reveal no more of a design than what shows up in data books.

A short definition of a complete and accurate model is that it represents all hardware registers by a model variable and includes full timing information. However, many storage-element models don't model timing. Thus, the more incompletely modeled storage registers you have in your design, the more accuracy problems you'll have. Parts that present the greatest modeling challenges include high-speed pipelined microprocessors and asynchronous logic such as disk-drive and SCSI controllers.

Because all storage elements consist of groups of gates, a gate-level model that includes timing is completely accurate. That's great for you as a designer—you can use the detailed functional information a gate-level model provides to extract greater speed and performance from a part. But that's bad for the part maker.

Beyond the possibility that you'll clone the part, the part maker acquires greater liability by releasing gate-level models and can inadvertently reveal future strategies for part development. For example, one company reports building a model for a disk driver from the hardware schematics. Simulations showed that the driver's maximum speed was twice the speed rating that its manufacturer published.

Because model accuracy and confidentiality hinges on how storage elements are represented, higher-level models can still pose a security risk to the part maker. Even behavioral models can disclose proprietary design information. Synthesis tools can automatically generate at least partial gate-level designs from behavioral models, says Bill vanCleemput, president of the Delos Research Group (Mountain View, CA), a company that specializes in intellectual-property work. Also—contrary to popular belief—VHDL can model at the gate level and handle hardware timing. It's entirely possible to make a VHDL model complete and accurate enough to reveal proprietary information.

Part makers usually restrict proprietary information by releasing only compiled, or object, code for complex models. The modeling team constructs the model to conform to data-book specifications, and the manufacturer does not release the model's source code.

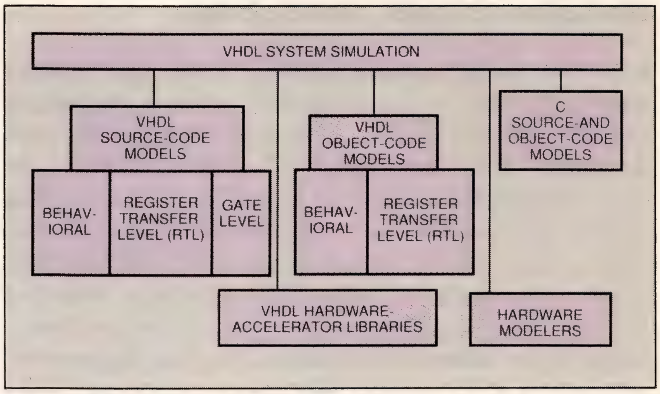
Logic Modeling Inc's recent release of its VHDL Sourcemodel Libraries gives an example of the dividing line between proprietary and nonproprietary information. The library includes VHDL source code for 600 SSI and MSI parts and 1400 simple memory devices but has no source code for LSI parts. The company released its Smartmodel Library only in object code. This library contains models for 6500 components including microprocessors, FPGAs, DSP μPs, and complex VLSI parts from leading semiconductor manufacturers.

In addition to the gate-level design, models can give away timing information. Foundries try to keep equations for timing calculations in-house because accurate equations reveal the strengths and weakness of a silicon process. If you push timing limits by using incomplete information, you may cause timing problems in your circuit. The accuracy limits of complex-part models often show up when an advanced user uncovers a problem by pushing a model's published limits. Foundries do help large-volume customers with such problems by giving them the information they need—as long as the customer agrees to sign a nondisclosure agreement.

chip itself. See EDN's Hands-On VHDL Project "Secrets of the Lost Architecture," which began in the January 7, 1993, issue.)

An example of currently available models for core-based design is LSI Logic's Coreware program for its 500,000-gate technology. The models include SPARC and Mips microprocessors, the MIL-standard 1750A CPU and IEEE-754-compliant FPUs, several ALUs and multipliers, and JPEG and MPEG chips. The company doesn't provide gate-level models. Instead, it makes fast C-language models that are functionally and timing equivalent to gate-level models. A C shell plugs these models into source code running on VHDL simulators from Vantage Analysis Systems and Synopsys as well as Verilog simulators from Vantage and Chronology Corp. You get only the compiled-code forms of these models.

The models Synopsys makes available for its VHDL System Simulator are another example of current practices. Under one of many agreements that Synopsys



The modeling levels used in VHDL system simulation span the full range of design abstraction. VHDL source models are available for SSI and MSI components. VHDL object models are sometimes available for LSI components, but they usually model only bus activity rather than all I/O. Hardware modelers are tools that interface working silicon with software simulators. Hardware-accelerator libraries group VHDL primitives to speed simulations. And the C language links VHDL simulators to user-built models and models for proprietary EDA toolsets.

VITAL team pursues VHDL timing standards

At last year's Design Automation Conference, Cadence Design Systems Inc initiated VITAL—the VHDL Initiative Toward ASIC Libraries. The group's goal is to create uniform formats for gate-level timing in VHDL. Such a standard would replace the dozens of approaches now used by semiconductor and EDA-tool vendors. Steve Schulz, North American coordinator for VITAL, says the effort now involves 40 companies worldwide representing a broad cross section of semiconductor vendors, EDA-tool suppliers, and ASIC designers.

The problem with VHDL is that the language isn't efficient at expressing pin-to-pin delays and performing setup and hold checks, says Stephen Caplow, director of marketing for VHDL at Cadence. The language's designers sought independence from specific silicon technologies, so they didn't define VHDL's timing primitives in such a way that they would map efficiently to a layout.

VHDL can represent any gate as text, thus making a large ASIC look like thousands of primitives. Each primitive generates a software process in VHDL, which consumes host-machine resources and makes simulations run slowly. VHDL accelerators—whether hardware or software—recognize a predefined set of primitives above the gate level. In other words, accelerators group gates together and run them as one process. Verilog includes such timing primitives, which gives it advantages over VHDL in gate-level simulation, timing checks, and carrying logical design to layout.

To standardize VHDL gate-level timing, VITAL plans to use the IEEE 1164 standard for defining signal strength and is considering using Cadence's Standard Delay File (SDF) format for timing information. Multiple tools, such as those for static timing and synthesis, could read an SDF. Existing foundry tools for calculating timing delays could store their results in the SDF. VHDL simulators could access this timing information during linking, or "elaboration."

Although VITAL's work began with gate-level timing, the group is also proposing a standard VHDL description for megafunction cells. Such a standard would make timing semantics portable across toolsets. Whether this proposal blossoms into a full treatment of multilevel-modeling issues remains to be seen. Fred Cohen, director of the ASIC vendor group at Mentor Graphics (Beaverton, OR), suggests that business issues outweigh technology issues when it comes to developing standards for ASIC multilevel modeling. But he encourages VITAL and VHDL International to accept the challenge, even though it's somewhat beyond the charter of either organization.

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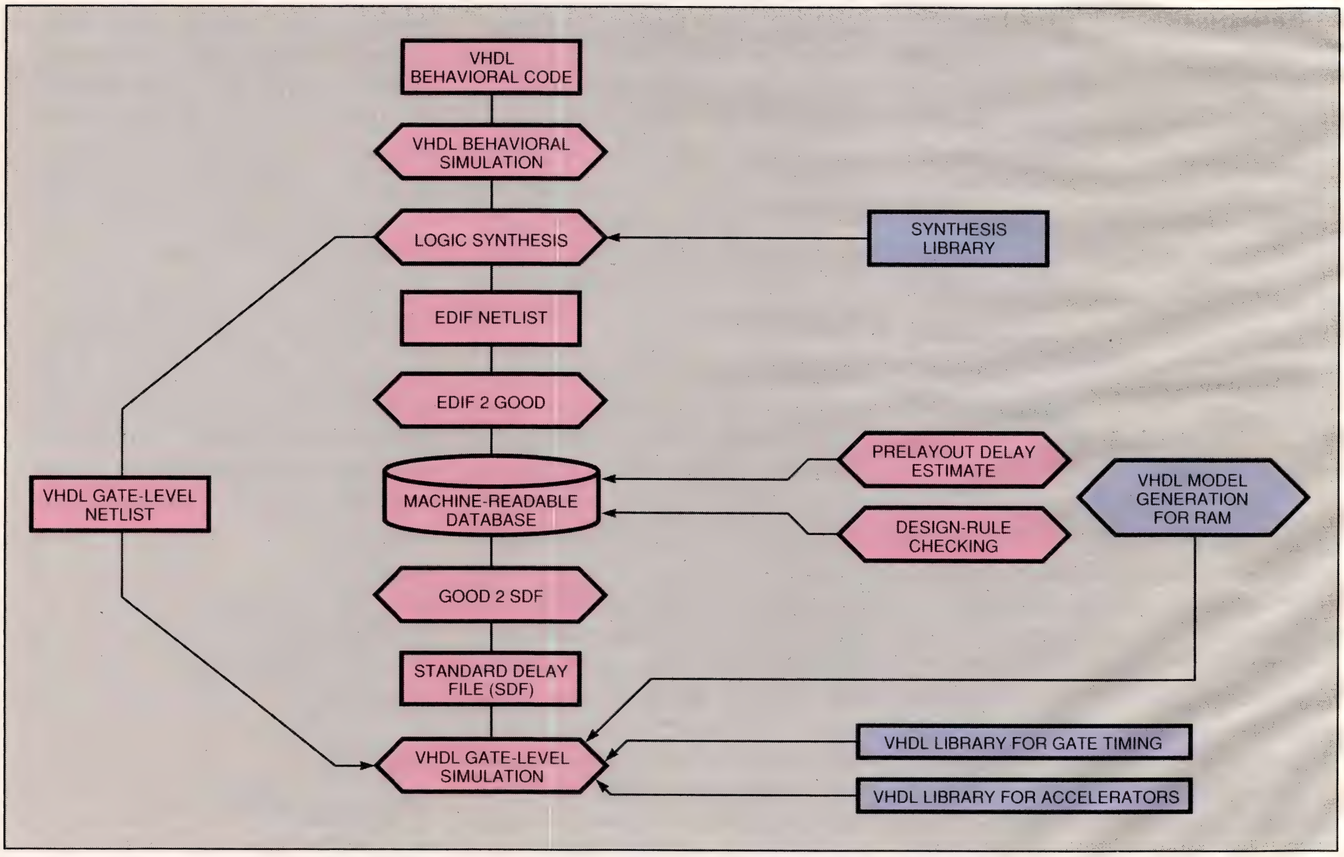
Multilevel ASIC modeling

has with ASIC manufacturers, Texas Instruments makes available to Synopsys four types of models for the TMS320 line of DSP μPs: a fast functional model for design validation; one that's timing accurate for cycle boundaries; a third for signoff by TI for building silicon; and the fourth, a synthesis timing shell that uses a subset of the signoff model with additions that cover drive-signal strength. The Synopsis simulator lets you view simulations as traditional low-level waveforms or as higher-level information. The higher-level simulations give you the information in the part data book, including instruction-level data and register and pipeline contents.

The hardware modeler is another aid to simulating systems before standards emerge for multilevel modeling. Combined with SSI and MSI (small- and medium-scale integration) models in source code and LSI models in object code, the hardware modeler lets you simulate boards or systems. The tool lets complex parts run at close to full hardware speeds within the much slower software simulation of a complete system.

Some complex ICs can't run in single-step mode, and therefore require you to use hardware modelers to connect the parts to software simulations. An example of a hardware modeler is the LM-1200 from Logic Modeling Inc. The product includes a blank cardrack, pattern memory, and software to interface parts to workstation-based simulators. You purchase cards and some peripheral circuitry to hold your part, and you write some driver code to interface your part to the modeler. The pattern memory saves data required to let the part run at speed and yet interface to the much slower software simulator.

If you want to build your own inventory of core models by reusing your previous work, look into Synopsys' Designware. The toolset provides structured methods for managing designs. The methods help you organize libraries of your own work and can compile reports on design characteristics. A companion product, Synthetic Designs, consists of synthesis and simulation models for advanced MSI logic, math, and sequential-processing designs in VHDL or Verilog. The combination of tools lets you focus on such issues as throughput and latency of an FIR



The burden of compensating for lack of VHDL timing information for multilevel modeling falls mostly on semiconductor vendors, as this synthesis-based VHDL design flow from Texas Instruments' Military Products Div shows. (Rectangular blocks show libraries and models; pointed blocks show tools.) The flowchart includes three TI-written libraries: a synthesis library that maps ASIC design components via a VHDL netlist to TI-specific gate; a second library passes the gates' timing characteristics to the VHDL simulator; and a third provides timing information for other primitives for hardware acceleration. A TI tool that generates models for RAM directly translates behavioral information into timing-capable simulation models.

Multilevel ASIC modeling

filter rather than designing the multiplier/adder for it.

Calls to semiconductor vendors revealed this general rule: More and better models become available the tighter you lock your design into a particular fab. Texas Instruments doesn't supply VHDL behavioral models. The company regards such models as its customer's responsibility, per Claude Huffer, military ASIC design engineering manager, and Dan Jensen, ASIC strategic marketing manager. The company does offer VHDL models for gate-level primitives and has the relationship with Synopsys Corp that facilitates core-based design with the TMS320 line.

Motorola made an MC68000 core model available last year for gate arrays. The Verilog model is proprietary, and Motorola judged the language's encryption techniques as too weak to protect the company's intellectual property. Motorola therefore teamed with a third party to make a C model for simulators. The Verilog C model comes in Verilog object format. It models function only; a Verilog "wrapper" file provides timing information. The 68000 model is not synthesizable, so you can't reduce an entire design to the gate level. The company has an effort underway to produce models for other parts in this family, but so far only the MC68000 core model is available.

VLSI Technology offers core models for the Z80, the ARM RISC processor 600 series, and a fuzzy-logic processor. The semiconductor vendor also has an agreement with Intel to supply 80386 microprocessor core models. You're required to make royalty payments to use any of these models.

Lastly, Fujitsu Microelectronics is looking into core-based design and expects in 12 to 18 months to have models available for some SPARC cores, SCSI controllers, and RAM and data-communications parts. The models will remain Fujitsu's intellectual property for use of its customers only, so you will not be legally able to take a netlist to make silicon at another fab.

A common industry belief is that models will eventually become a byproduct of hardware development. That's unlikely to happen for two reasons. First, the part maker needs to protect design ownership and limit liability. Second, making models is labor-intensive software-development work and represents overhead to the main business of making chips.

You also can't count on the aging of patents to put complex parts in the public domain anytime soon. Patents last for 17 years, and trade secrets last as long as a company protects them. Models are readily available for MSI parts because many of these parts are so simple that they're not patentable. Others have been around so long that they're in the public domain. Today's complex LSI parts will probably become technically obsolete long before their 17 years are up. EDN

References

1. *VHDL Design Guide*, Cadence Design Systems Inc, 1992.
2. *Handbook of Hardware Modeling*, Logic Modeling Inc, 1991.

Article Interest Quotient (Circle One)
High 497 Medium 498 Low 499

Manufacturers of simulation tools and models

For more information from suppliers of tools and models such as those mentioned in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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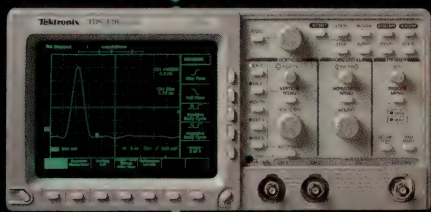

Tektronix

CIRCLE NO. 35

ICs provide control for sensorless dc motors

Dave Peters and Jeff Harth, Silicon Systems Inc

The need for low-cost, highly reliable, miniature, brushless dc motors has given rise to a new class of devices—sensorless dc motors. These motors eliminate the need for Hall-effect sensors, which are currently built into most brushless dc motors for control purposes.

As dc motors get smaller, there is less space for the Hall-effect sensors you normally use for motor control. As a result, miniature sensorless motors are becoming common. Eliminating the Hall-effect sensors removes the need for sensor-control signals, reduces the size of the connector, and eliminates connections. Hall-effect sensors are also sensitive to temperature variation, RFI, and other types of noise commonly experienced in motor applications. All of these factors reduce motor reliability. Finally, Hall-effect sensors increase motor cost and make the motors larger. As a result, the motors consume power—an undesirable trait in battery-driven applications.

While eliminating Hall-effect sensors obviously has its advantages, it also has some disadvantages. Without Hall-effect sensors, brushless dc motors are somewhat more difficult to start and control. Fortunately, a variety of semiconductor manufacturers now offer ICs that are specifically designed to control sensorless dc motors. These chips monitor the back-EMF the motors generate across specific sets of windings and appropriately adjust the amplitude and polarity of the voltages across the motor windings. In this manner, the ICs switch the motor from one commutation state to the next in a programmed manner, automatically setting and regulating the speed.

In addition to speed control, you should also consider the question of motor starting. Starting is a unique problem for the sensorless motor, because back-EMF exists only when the motor is already turning. For start up to occur, the motor must rotate in the proper direction and attain a speed that lets back-EMF sensing begin. Today's sensorless motor-controller chips switch the amplitude and polarity of the voltages across the motor windings so that the motor starts turning slowly and then accelerates, in a programmed manner, to a speed where back-EMF speed control can take over.

If start up always involves identical conditions, you can preprogram a single self-start acceleration profile

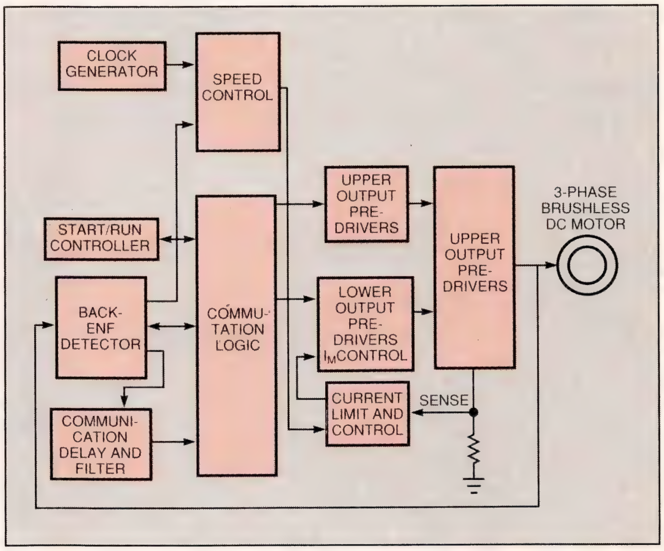

Fig 1—The speed-controller chips available today provide all the timing and control functions necessary to control speed, drive, and brake 3-phase, multipole brushless dc motors.

for the motor. If the load or other conditions will vary, start up may require adaptive microprocessor control. In this case, the μP will adjust the start profile to begin with the unknown load.

You can control motor speed by varying the current in the motor windings. You can vary the current in a linear fashion by varying the voltage applied to the windings, or you can use pulse-width modulation (PWM) techniques and keep the voltage constant.

PWM-control techniques typically vary the duty cycle of the voltage applied to the motor windings to control the current in them. PWM control is most appropriate in applications where low power dissipation is very important. You vary the current to each winding by switching a power transistor on and off at a variable rate, or at a fixed rate with a variable duty

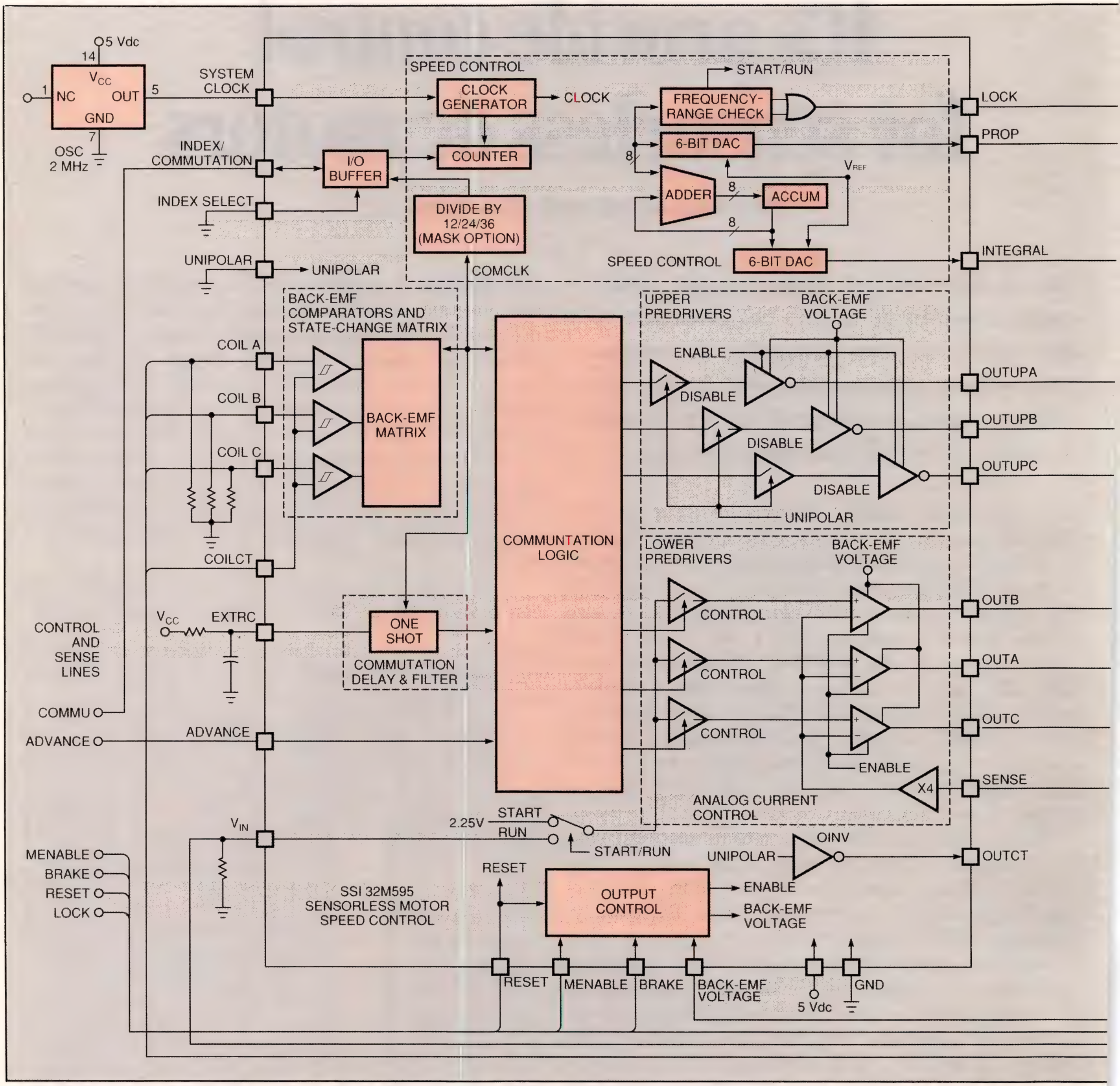

Fig 2—The current-limiting resistor R_{SENSE} is a key component in the sensorless motor-controller circuit. The resistor limits the start current to the motor windings and should be chosen to allow a start-up current about 10% higher than what is required.

cycle. Unfortunately, PWM-control schemes are more difficult to implement than linear schemes.

For either speed-control method to work, the controller must receive an index pulse, which indicates the start of a motor revolution. There are two ways to generate this index pulse. You can use an external optical shaft encoder to generate the pulse, or you can use the on-board speed controller or an external μP to flag the start of a motor revolution by counting changes in commutation states. A 3-phase motor has six commutation states for each pair of poles. Once the μP knows how many pairs of poles the motor has, it can calculate the number of changes of commutation state in one revolution of the motor. It then simply counts changes of commutation state for each revolution and knows precisely when a new revolution is beginning.

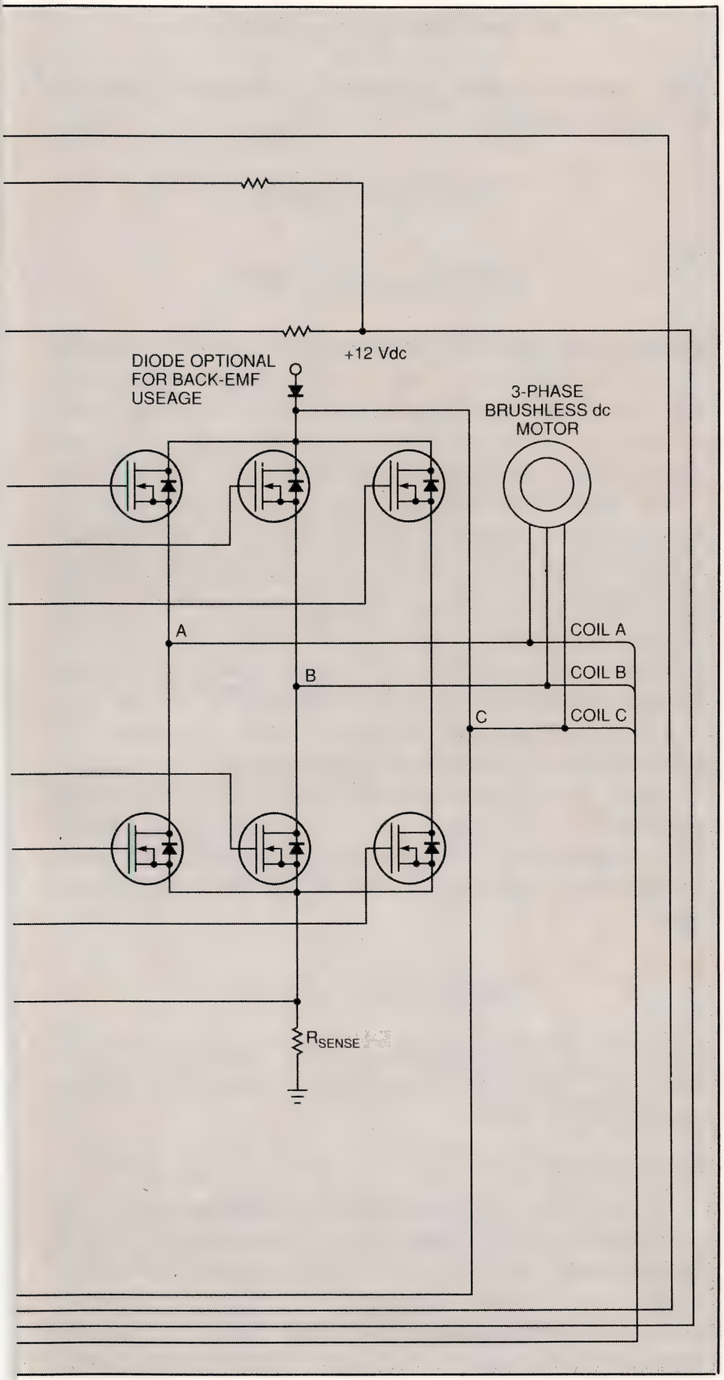

Fig 1 illustrates the basic system for brushless dc-motor control. This generalized system appears in two specific examples—one involves the control of a 12V bipolar motor and the second deals with a 24V unipolar motor. Both examples use the SSI32M595 sensorless motor-speed control chip—a device that contains on-board speed control. However, other products on the market can do a similar job.

The bipolar approach has the advantage of providing greater torque with the same motor design, while the unipolar scheme allows higher rpm, because all the voltage develops across a single winding. In addition, the unipolar design requires only one power transistor per terminal. However, it also requires a voltage divider circuit at each terminal to bring the voltage to the 12V range.

Solving disk-drive problems

A disk-drive application using a sensorless motor as the spindle motor best typifies the task of 12V bipolar motor control. Assume that the drive has four 3½-in. disks and eight read/write heads. The disks rotate at 3600 rpm (377 rad/sec), and the spindle motor must get the disks up to the speed where the heads fly within 2 sec. The heads start in contact with the disk surfaces, yielding 15g of head load and a friction coefficient of about 1. At a speed of 1000 rpm, the heads start to fly.

Estimating the system inertia is the first step in the design. If you assume that motor inertia is small compared to disk inertia (a valid assumption in most cases), then system inertia will be equal to disk inertia. Assume that disk inertia equals 0.0075 oz-in.-sec^2 in this case. Calculating torque requirements is the next step. The acceleration rate (α) necessary to get up to 1000 rpm (104.7 rad/sec) in 2 sec equals the speed divided by the time to reach that speed, or $104.7/2 = 52.35$ rad/sec^2. The torque (T) required to accelerate the inertia equals the system inertia (estimated earlier to be 0.0075 oz-in.-sec^2) multiplied by the acceleration rate α, or

$$T = 0.0075 \times 52.35 = 0.393 \text{ oz-in.}$$

To overcome the head friction at start-up, you must

add an additional torque element, T_F. Assuming a head-park radius (distance from center of the disk to the track location where the heads are parked) of 0.55 in., then T_F will equal

$$(15g/28.35)(8)(1)(0.55\text{ in.})=2.3\text{ oz-in.},$$

where 15g equals the head load, 28.35 equals the metric-to-English conversion factor, 8 equals the number of heads, 1 equals the coefficient of friction, and 0.55 equals the head-park radius. The total starting torque required is the sum of T and T_F, or 2.69 oz-in.

Take a worst-case approach

To calculate the starting current for the motor windings, you must first calculate the motor-torque constant. To reflect worst-case conditions in a 12V system, assume a value of 10.8 for the low-line condition. Allowing 3V for head room to control speed means that the motor's back-EMF should be no more than 7V. Thus, the torque constant, K_T, will be

$$(7/377)141.6=2.63\text{ oz-in./A},$$

where 377 equals the disk rotation in rad/sec and 141.6 is a factor that converts (volt-sec)/rad into oz-in./A. This is the probable upper limit to K_T and is meant to serve as a first approximation. Dividing the total starting torque ($T + T_T$) by the torque constant gives the start-up current for the motor windings as 2.69/2.63 = 1.02A.

Fig 2 details the control scheme for the 12V bipolar sensorless motor application. Note that the schematic includes a current-limiting resistor (R_{SENSE}) that limits the start current to the motor windings. Select a value for R_{SENSE} that allows a start-up current about 10% higher than necessary. In this example, the current limit is equal to 2.25 (the chip's internal acceleration voltage) divided by $4R_{SENSE}$. If R_{SENSE} is equal to 0.5Ω, the current limit works out to 1.125A.

At this point, you can calculate the elements of a start-up table. This table is a list of delay times between advances to the commutation state counter that allow time for the motor to rotate to the location where the next advance should occur. For a typical 3-phase, 8-pole motor, the angle of rotation per state is

$$\theta=2\pi/(3)(8)=0.262\text{ rad/state}.$$

The amount of time required to complete a rotation of angle θ is either

$$(\omega_{(N-1)}+\omega_N+\alpha T_N/2)T_N,$$

or

$$(\alpha TN^2)/2+\omega_{(N-1)}T_N-\theta+0,$$

where T_N is the time to move through an angle of θ in a time period of N; $\omega_{(N-1)}$ is the angular velocity at the end of the last time period and at the start of the N time period; ω_N is the angular velocity at the end of the N time period; and α is the angular acceleration.

You must now calculate α at the current limit I_M. The torque produced equals $I_M K_T$, which equals 1.25A × 2.63 oz-in./A = 2.96 oz-in. The amount of torque available for acceleration is the torque produced at the current limit less T_F, or 2.96 − 2.3 + 0.66 oz-in. The acceleration rate α equals the torque available for acceleration divided by inertia, or 0.66/0.00785 = 88 rad/sec^2.

You can enter this value of α into the quadratic equation for the amount of time to complete a rotation of angle θ and then solve the equation to determine time per step. The first step, where the previous velocity is zero, is starting the motor from a dead stop. When solving the equation for N = 1 and θ = 0.262 rad/state,

$$(88/2)T^2+0T-0.262=0,$$

the time (T) to complete the first step of θT equals 0.077 sec, and the instantaneous rotational velocity equals 6.79 rad/sec.

Get a computer

You can use a simple computer program to run this calculation and generate a table. The number of steps in the start table must bring the motor above the speed where reliable commutation will occur. Then, the start cycle will end and self-commutation will take control. Assuming that the target speed is 500 rpm, a table for the design in **Fig 2** will require only about 60 steps (**Table 1**).

The next task is to calculate the maximum motor re-

Table 1—Motor start up

Interval	T (msec)	T total (msec)	rpm
1	77.2	77.2	64
2	31.98	109.19	91
10	12.52	244.15	204
20	8.74	345.29	289
30	7.1	422.89	354
40	6.14	488.31	409
50	5.48	545.95	457
59	5.04	593.05	497
60	5.0	598.06	501
61	4.96	603.02	505
70	4.63	645.97	541

sistance, R_M. The total available low-line power-supply voltage is impressed across three components—the driver transistors, the current-sample resistor, and the motor. The motor-terminal voltage is simply the back-EMF plus the IR drop across the motor resistance. There are two power transistors driving each motor winding in a bipolar application. Assume that the voltage drop will be the same across each transistor.

For a current of 1.125A (the current at start-up), the voltage drop across both transistors will be about 2V. The voltage drop due to motor resistance, V_{RM}, equals the low power-supply-voltage level minus the back-EMF (which is zero at start) minus the voltage drop across the driver transistors less the voltage drop across the sense resistor. Thus, V_{RM} works out to be $10.8-0-2-(1.125\times 0.5)=8.24V$. Since $V_{RM}=I\times R_M$, R_M will equal $8.24/1.125=732\Omega$.

The values for K_T and R_M are a good approximation for a design start. Having some values for K_T and R_M (two key motor specifications) lets you move on to the next step—setting the speed-control compensation. A 2-MHz system clock sets the internal speed control for 3600 rpm. External resistors (between the proportional-error DAC, the integral-error DAC and V_{IN}, and the summing resistor from V_{IN} to ground) provide the compensation for the speed-control loop.

You can determine the required values for the gain-control resistors needed to complete the speed-control compensation design by solving the loop-gain equations. The loop-gain control equation is

$$LG=(11.6K_IK_AK_T/js^2)+(0.775K_PK_AK_T/js),$$

where LG is the speed-control loop gain; K_I is the integral gain set by the external resistor (R_I) in the network; K_P is the proportional gain set by the external resistor (R_P) in the network; K_A is the current-control transconductance gain $=1/(4R_{SENSE})=0.5$ A/V; K_T is the motor torque constant $=2.63$ oz-in/A; J is the inertia $=0.0075$ oz-in.-sec^2; s is the LaPlace Transform frequency variable, which $j\omega$ can replace.

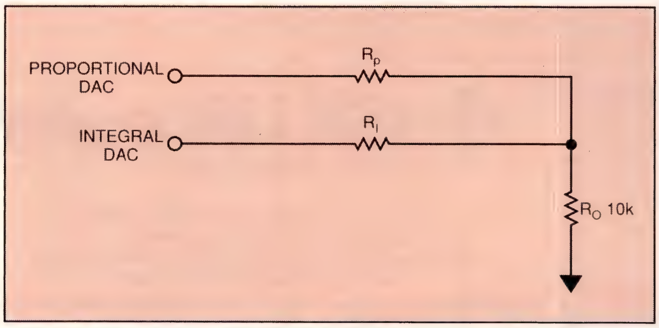

Fig 3—The compensation for the speed-control loop is done with external resistors between the proportional-error DAC, the integral-error DAC, and V_{IN}, with an additional summing resistor located between V_{IN} and ground.

For 45° phase margin when the loop gain equals 1.0, the loop-gain in rectangular form is

$$-0.707-j0.707=(11.6K_IK_AK_T/j\omega^2)-j(0.775K_AK_TK_P/j\omega).$$

Assume you want a 1-Hz bandwidth, then you must solve the above equation when $\omega=2\pi(1\text{ Hz})$. Solving the real and imaginary parts separately for K_I and K_P yields values of $K_I=0.0132$ and $K_P=0.0327$. **Fig 3** shows the network that will produce these gains, where $R_O=10$ kΩ, and R_P and R_I are the gain control resistors:

$$R_P=R_O(1-K_I/K_P)-1=291.6\text{ k}\Omega$$

and

$$R_I=R_O(1-K_P/K_I)-1=695\text{ k}\Omega.$$

This ends the design process for the circuit in **Fig 2.**

Handling unipolar applications

To illustrate the design process for sensorless motor control in unipolar motor applications **(Fig 4)**, consider the following design problem. The application here requires a variable speed control with an external speed sensor and controller, using a sensorless dc motor. The input for the speed control is the transconductance input V_{IN}. Load inertia plus motor inertia will be 0.01 oz-in.-sec^2, and speed control is required over a 1000-to 10,000-rpm range. Speed must be capable of changing from the low speed to the high speed in 1 sec. In this case, assume that you have negligible friction torque or viscous torque to deal with. Also, the motor is a 3-phase, 4-pole wye-connected motor, with center tap, as in the 12V bipolar example.

To operate in a unipolar fashion at greater than 12V, you must develop voltage divider networks for each of the motor's terminals, since the control chip should never have more than 15V on any input. In addition, you must bypass the motor-controller chip's internal low-rpm switch so that it will not switch motor current control away from V_{IN} to the internal acceleration voltage (2.25V). This circuitry provides full acceleration if the speed is very low compared to 3600 rpm (the nominal fixed motor speed used in disk-drive applications).

With a 2-MHz clock and an 8-pole motor, the low-rpm switch will activate if the rpm drops below 3492. To bypass the low-rpm switch, select a new clock frequency, which is a function of the number of poles in the motor and the motor's lowest operational control

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CIRCLE NO. 94

speed. The formula for the new clock frequency is

$$F_C = (\text{number of poles}/8)(\text{low rpm}/3492)(2\ \text{MHz}).$$

Because the number of poles is four and the low rpm is 1000, the new clock frequency will equal 286 kHz. The resistor-divider network, connected to the motor windings, is shown in **Fig 5**. The maximum voltage at A, B, and C equals the supply voltage plus the back-EMF.

The acceleration rate necessary to reach full speed in 1 sec places a torque requirement on the motor. You can calculate this torque by multiplying the acceleration (from 1000 rpm to 10,000 rpm in 1 sec) by

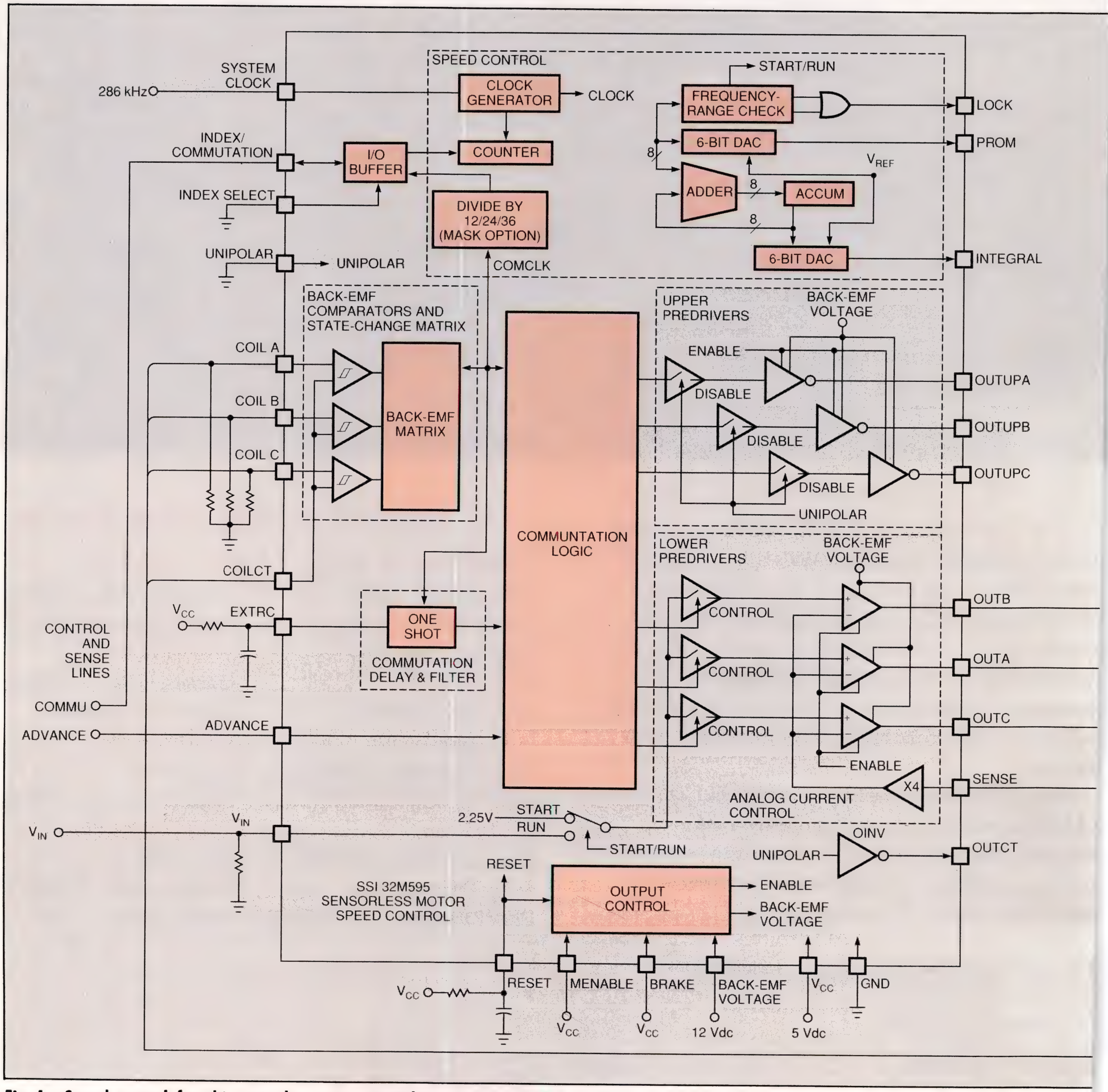
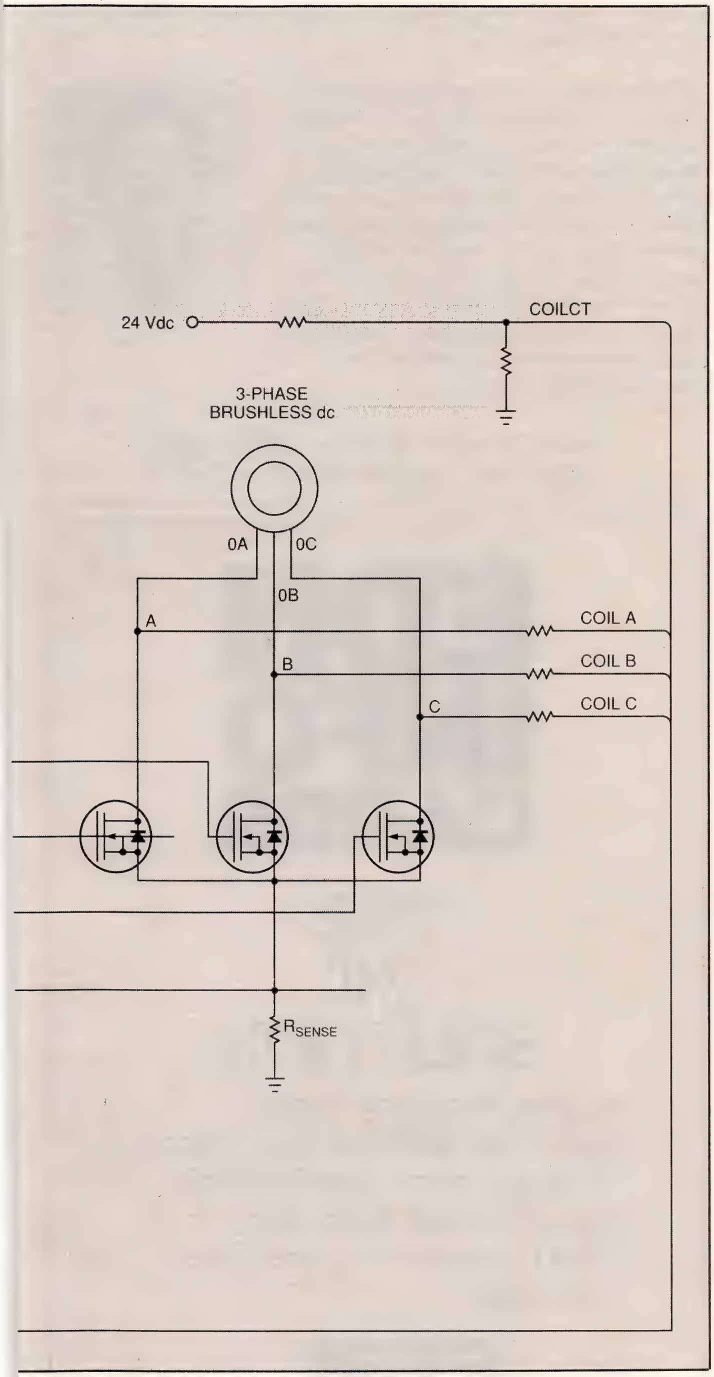


Fig 4—Speed control for this unipolar motor-control circuit is provided at the transconductance input, V_{IN}. In this case, the motor is again a 3-phase, 4-pole wye-connected unit with a center tap.

inertia. Because the acceleration required is 942.5 rad/sec^2, and the inertia is 0.01 oz-in.-sec^2, the torque required is 9.425 oz-in.

Torque constant is a function of the amount of back-EMF the system can handle at maximum speed and the motor-winding resistance. The total voltage available is 24V. This voltage drops across the back-EMF, the driver transistor, and the motor winding. Maximum back-EMF occurs when the motor is spinning at 10,000 rpm (1047 rad/sec). Therefore, the back-EMF is related to the torque constant K_T by $(K_T/141.6)(1047$ rad/sec) and equals $7.394K_T$.



You can determine the IR drop in the motor windings (R_M) and R_{SENSE} by dividing the motor torque by the torque constant and multiplying the result by the sum of the motor-winding resistance (R_M) and R_{SENSE}. To calculate V_{SAT}, the voltage dropped across the driver transistor, divide the motor torque by the torque constant and multiply the result by the effective resistance (R_{DSON}) of the driver transistor—0.3Ω, in this case.

The voltage applied across the motor terminals in **Fig 4** is equal to the back-EMF ($7.394K_T$) plus the IR drop in the motor windings $(9.425/K_T)(R_M+R_{SENSE})$ plus V_{SAT} $(9.425/K_T)R_{DSON}$. Therefore, 24V − back EMF − IR − $V_{SAT}=0$ is a limit for K_T and R_M. Let $R_T=R_M+R_{SENSE}+R_{DSON}$. Therefore,

$$24-7.39K_T-(9.425/K_T)R_T=0.$$

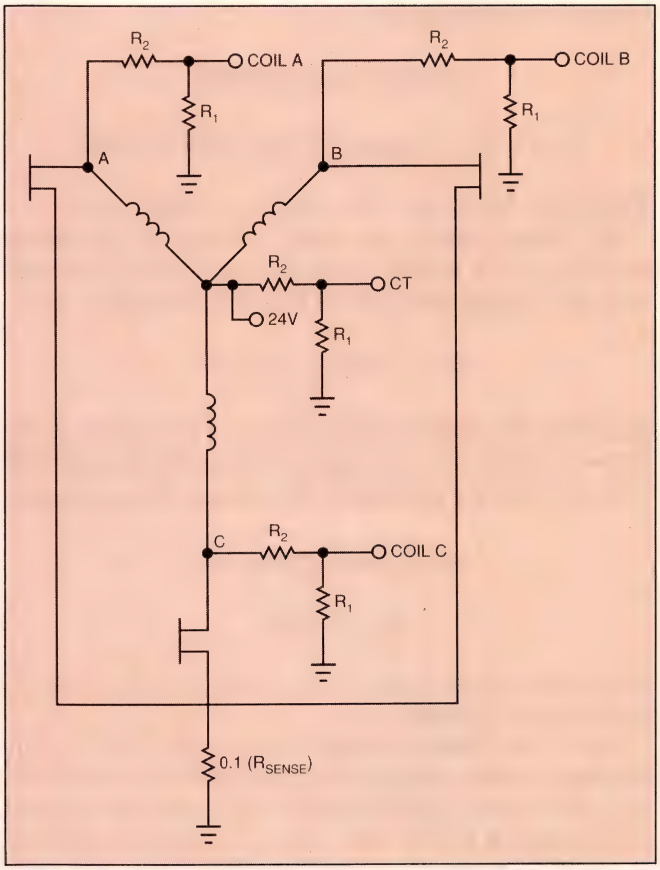


Fig 5—To operate in a unipolar fashion at voltage levels greater than 12V, you must develop voltage-divider networks for each of the motor's terminals because the control chip should never have more than 15V on any input.

MOTOR SPEED CONTROL

Now you rewrite the equation to solve for K_T as

$$7.394\ K_T2 - 24K_T + 9.425R_T = 0.$$

You can assume a value for R_T and solve the quadratic equation K_T. If the roots are real, K_T can take the higher value and R_T can assume the trial value. To find the highest possible value for R_T, iterate to find the point where the roots for K_T are real and nearly equal to each other. The iteration yields an R_T of 2.065Ω and a K_T of 1.66:

$$R_T - R_{DSON} = R_M + R_{SENSE} = 2.065 - 0.3 = 1.765\Omega.$$

The current requirement through the motor windings will be equal to

$$9.425/K_T = 9.425/1.66 = 5.68A.$$

The value of R_{SENSE} will be equal to the voltage level at the current limit divided by the internal gain of the sense amplifier times the current requirement through the motor windings, or

$$2.25/(4 \times 5.68) = 0.099\Omega.$$

$$R_M = 1.765 - R_{SENSE} = 1.765 - 0.099 = 1.666\Omega.$$

Therefore, $K_T = 1.66$ oz-in. and $R_M = 1.666\Omega$ max.

For these values, the peak voltage at the motor terminals is the voltage drop across the motor windings plus the voltage drop across the driver resistor, or

$$24 + 7.394K_T = 36.274V.$$

To divide this peak voltage down to 12V or less at the motor winding, a you'll have to use a divider network such as that shown in **Fig 5**. You can use the expression

$$36.274(R_1/R_1 + R_2) = 12$$

or,

$$R_2 = 2.023R_1$$

to calculate R_1 and R_2. If R_1 equals 1.8 kΩ, then R_2 would equal 3.64 kΩ.

V_{IN} is the input to control speed and 2.25V is the maximum input voltage. V_{IN} controls the motor current, which can control speed. You need an external speed monitor in this case. The transconductance from V_{IN} to I_M is $1/(4R_{SENSE})$ A/V. Having calculated values for the voltage divider and motor parameters K and R, you have completed the design of the 24V unipolar senseless dc motor controller. EDN

Authors' biographies

Dave Peters is a consultant at Silicon Systems Inc in Tustin, CA. He gives seminars and workshops in servo-system and speed-control design. He was also a member of the team that developed the speed-control chip used in the design examples in this article. Dave attended Brigham Young University in Provo, UT and National University in San Diego, CA.

Jeff Harth is a principal applications engineer at Silicon Systems Inc. In this position, he provides technical design support for servo- and motor-speed-control products. Jeff was also a member of the team that designed the speed-control chip used in this article. He holds a BSEE degree from California Polytechnic State University (San Luis Obispo, CA) and a Master's degree in system engineering from West Coast University (Los Angeles, CA).

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MPI-650-10 THROUGH MPI-650-230	650 ---- 650	10Vct. @ 65.0A ---- 230Vct. @ 2.8A	5V @ 130.0A ---- 115V @ 5.6A	145.00
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Mechanical Dimensions

Size	L	W	H	ML (mtg)*	MW (mtg)*	WGT
200VA	3.750" 95.3 mm	4.203" 106.6 mm	3.720" 94.5 mm	3.250" 82.6 mm	2.800" 71.1 mm	6.22 lbs 2.82 kg
250VA	4.125" 104.8 mm	3.898" 99.0 mm	4.000" 101.6 mm	3.625" 92.1 mm	2.601" 66.1 mm	6.76 lbs 3.07 kg
300VA	4.125" 104.8 mm	4.223" 107.3 mm	4.000" 101.6 mm	3.625" 92.1 mm	2.915" 74.0 mm	7.80 lbs 3.54 kg
400VA	4.125" 104.8 mm	4.805" 122.0 mm	4.000" 101.6 mm	3.625" 92.1 mm	3.505" 89.0 mm	9.82 lbs 4.46 kg
650VA	5.250" 133.3 mm	4.430" 112.5 mm	4.800" 121.9 mm	4.500" 114.3 mm	3.415" 86.7 mm	14.83 lbs 6.73 kg
900VA	5.250" 133.3 mm	5.197" 132.0 mm	4.800" 121.9 mm	4.500" 114.3 mm	4.205" 106.8 mm	19.84 lbs 9.01 kg

Part No.	VA	Secondary Series	Secondary Parallel	1-9 Pcs Price
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HPI-35	3500	230V @ 15.2A	115V @ 30.4A	450.00

Mechanical Dimensions

Size	L	W	H	ML (mtg)*	MW (mtg)*	WGT
2000VA	7.500" 190.5 mm	5.600" 142.2 mm	6.560" 166.6 mm	5.750" 146.1 mm	4.350" 110.5 mm	41.3 lbs 18.71 kg
2750VA	7.500" 190.5 mm	6.230" 158.2 mm	6.560" 166.6 mm	5.750" 146.1 mm	4.980" 126.5 mm	48.0 lbs 21.77 kg
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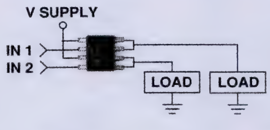

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dual p-ch	-12	0.21 @ V_{GS}= -2.7V	±3.0

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CIRCLE NO. 111

The little modem that could

Think of all the digital sorts of things that you'd like to do with your standard phone line: high-speed data communications, caller ID, and fax transmission and reception. Now envision these capabilities realized in a small, 1-in.-high aluminum box. What you see in your mind's eye is the 14.4-kbps Supra FAXModem V.32bis, a reliable workhorse for computer communications over the telephone. The external version of this product costs $399.95. The company sells this product with DOS- or Windows-based communications and fax software for $449.95, $389.95 for an internal package, or $479.95 for a similarly equipped Mac package.

I've owned a Supra 2400-bps modem for many years. It always operates reliably, even over noisy phone lines. The FAXModem V.32bis retains this critical feature, despite the way I'm using it. You see, in EDN's modern office environment, we have no archaic analog phone lines. Instead, we have modern AT&T digital PBX lines, incompatible with all conventional telephone equipment. Thus I must use a special phone coupler from Konexx (San Diego, CA) that taps into my digital phone's analog handset cord and provides a convenient RJ-11 jack for a modem. Despite the Konexx box, the PBX's digitization of the modem signal and conversion back to analog, and the usual telephone system noise, this modem had no problems communicating with modems across the country.

The FAXModem V.32bis operates at speeds to 14,400 bps when talking to a compatible modem. If you want to save $100, you can buy the FAXModem V.32 for $299.95. Using the FAXModem V.32bis's MNP 5 data compression, you can theoretically achieve 38,400-bps transmissions, and BTLZ compression can take you to 57,600 bps. I never operated at those rates. You must be communicating with a compatible modem to use such high rates.

Beyond transmission rates, there's little you can say about a good modem; you plug it in, and it works. One unusual feature on this modem is a 2-character alphanumeric display that tells you what's happening with the modem. It tells you when the modem is dialing a number, when the remote modem connects with yours, and what transmission speed you're using. Being able to monitor this display is an excellent justification for having an external modem. The manual is clear, has several useful appendices, and includes a well-written troubleshooting chapter, on the off chance that you have problems.

Supra has updated the firmware in this modem twice since I received it. The first time was to expand the modem's fax capabilities. The product incorporates Rockwell's fax/modem chip set, so its capabilities are programmable. I tried the DOS-based fax software and easily was able to send a document to EDN's dumb fax machine but not to EDN's super smart "fax machine from hell" (EDN, October 1, 1992, pg 33). I didn't try to receive faxes using this modem because the Konexx box doesn't allow the modem to answer the phone. However, the fax abilities are really determined by the fax software. Supra provides Faxtalk from Thought Communications (Santa Clara, CA) for DOS faxing and Winfax from Delrina Technology (San Jose, CA) for Windows users.

The second ROM upgrade added caller-ID abilities to the modem. You could use this feature to screen calls, assuming that you don't have a PBX that filters such information from your phone lines, but another suggested use really caught my eye. Bulletin boards conceivably can use caller ID for automatic log in. However, this feature isn't much help for road warriors with laptop computers who call in from the nearest pay phone.

In summary, this is a modem that performs well. It has good documentation, it has state-of-the-art capabilities, the vendor supports it well, and it doesn't cost as much as many of its competitors. If there's anything more you could possibly want in a modem, it will probably appear in the FAXModem's next ROM upgrade.—**Steven H Leibson**

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DIGITAL ASIC ENGINEERS Requires a BS/MS in CS, EE or related science, plus a minimum of 5 years designing digital CMOS circuits. Must be familiar with digital signal processing in telecommunications applications, low power design methodologies, design for testability and FPGA prototyping techniques. Should have experience with modern design tools (VHDL, Mentor, Synopsys) for top down design simulation and verification.

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Mechanical Engineer

This position involves the physical design and development of electronic PWB assemblies and associated sheetmetal and plastic enclosures. As a member of an interdisciplinary product team, your responsibility will include thermal design, chassis design and PWB layout design. The successful candidate will have a BSME with at least 3 years of experience. Familiarity with UL, CSA, and VDE safety agency requirements a plus.

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Engineering support of ferroresonant product for use in telecommunication systems. You will provide sustaining engineering support for power supply product in full-scale production with continuous quality improvement and technical consultation with customers. Circuit design skills are required along with experience in magnetics, packaging, EMI, Bellcore requirements and strong analytical abilities. BSEE with 5 years of experience required.

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Interest and experience in test development including fixturing, documentation and software. experience with BASIC, C, UNIX, DOS, IEEE-488/HP1B and GenRad test equipment desired. Familiarity with power equipment and development desired. BS or MS degree in Electrical Engineering required.

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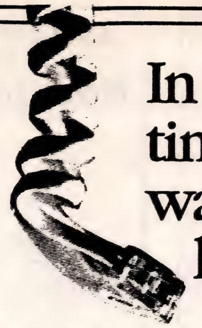

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Senior, mid and junior level Designers/Implementers with experience in "C" and Assembler on DOS PC and/or embedded microprocessors for real-time applications. Experience with communications systems highly desirable. Minimum three years of experience.

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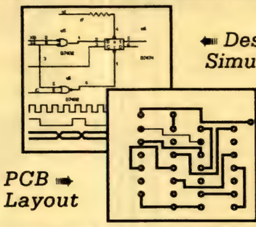

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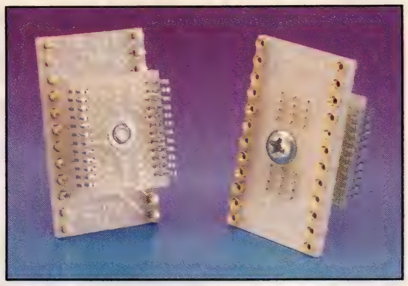

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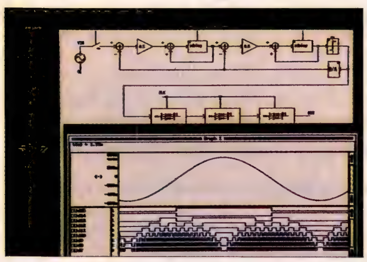

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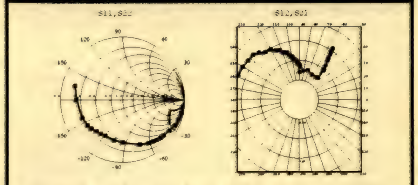

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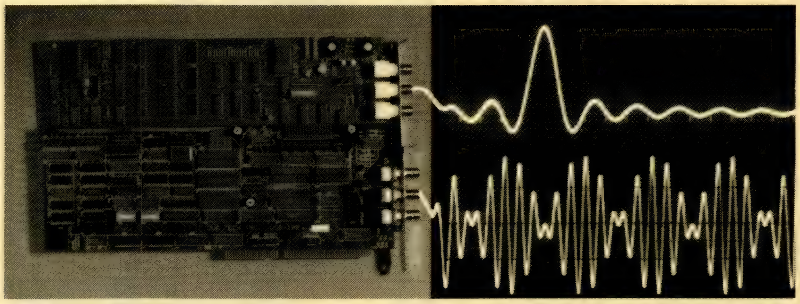

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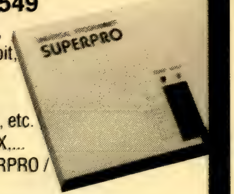

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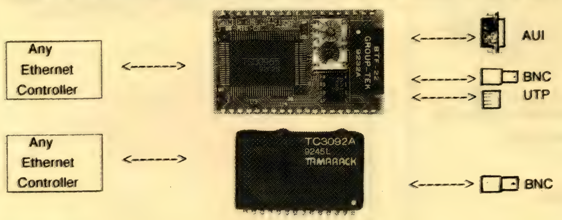

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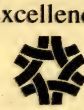

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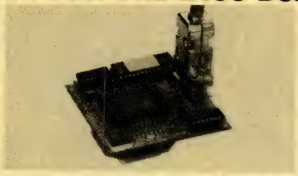

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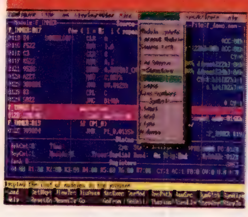

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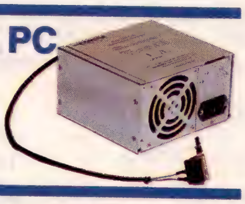

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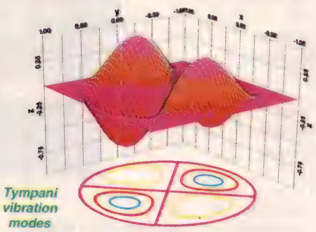

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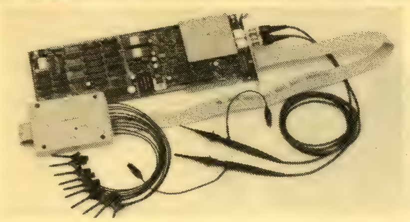

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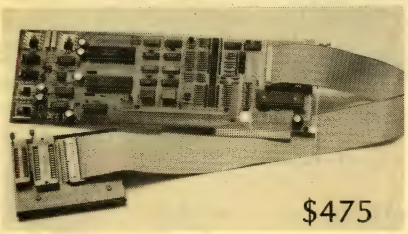

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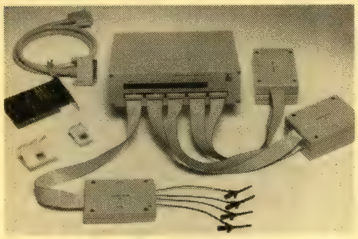

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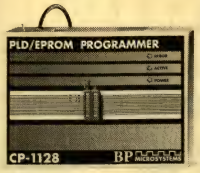

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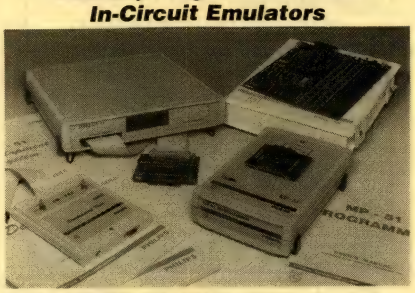

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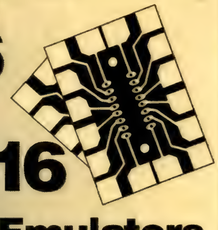

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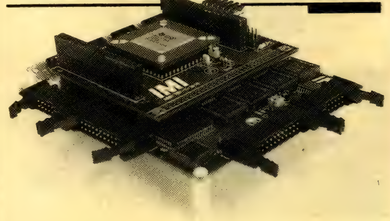

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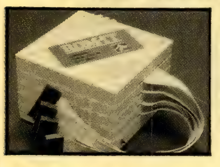

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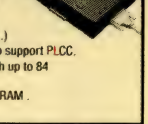

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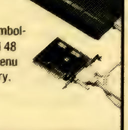

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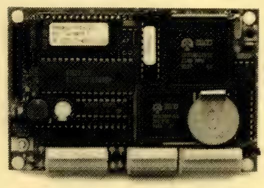

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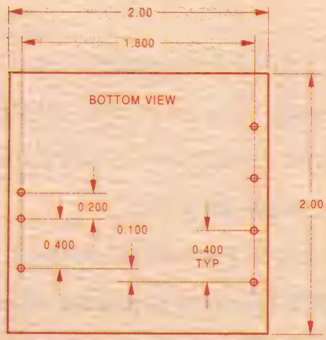

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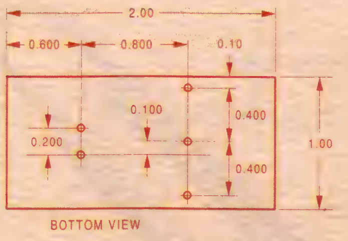

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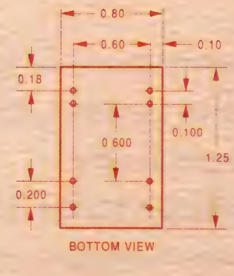

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Component information system. The added features of CIS 1.1 to the previous version include a user-configurable interface for customizing search and results windows; enhanced integration with CAE tools for improved searches; operation with all features of military components; enhanced comparison of components; and better management of in-house data and documentation from third-party sources. CIS 1.1 runs in client-server mode on Unix workstations. $50,000 to $250,000, depending on number of authorized users. **Aspect Development Inc,** 4410 El Camino Real, Suite 208, Los Altos, CA 94022. Phone (415) 941-2525. Fax (415) 941-9757. **Circle No. 466**

to assist with loading and testing CFI DR-compliant databases, and a development test for the DR-PI. Single-user license, $6000; unlimited site license, $30,000. **CAD Framework Initiative Inc**, 4030 W Braker Lane, Suite 550, Austin, TX 78759. Phone (512) 338-3739. Fax (512) 338-3853. **Circle No. 458**

Timing-driven crosstalk-analysis tool. DF/Signal Integrity is a timing-driven crosstalk-analysis product for designers of multichip modules (MCMs) and pc boards. It does not assume, as other tools do, that adjacent signals switch simultaneously. The tool enhances the crosstalk-driven routing capabilities of Cadence's Allegro Physical Design System. It runs on Unix workstations from vendors that include DEC, HP, IBM, and Sun. $21,000 to $45,000, depending on configuration. **Cadence Design Systems Inc**, 555 River Oaks Parkway, San Jose, CA 95134. Phone (408) 943-1234. Fax (408) 943-0513. **Circle No. 459**

Real-time OS kernel. Release 2.5 of the C Executive, a ROMable, multitasking OS kernel for real-time embedded systems, will run on 80386 and 80486 μPs. Control can pass from DOS to the C Executive, and from the C Executive to DOS, without rebooting. A standard PC can serve as a development system and a prototyping system. Price of the kernel depends on type and quantity of application. **JMI Software Consultants Inc**, Box 481, 904 Sheble Lane, Spring House, PA 19477. Phone (215) 628-0840. Fax (215) 628-0353. **Circle No. 460**

Image-development tools for Windows. Glide, an image-analysis software-development package, includes a library of imaging functions plus prototyping and debugging tools. It lets you create prototypes, without programming, within a Windows application. It then generates C code to execute your prototype functions. The package includes Global Lab Image, an image-analysis application program, and a companion dynamic link library (DLL). $3495. **Data Translation Inc**, 100 Locke Dr, Marlboro, MA 01752. Phone (508) 481-3700. Fax (508) 481-8620. **Circle No. 461**

JPEG image-compression ASIC core. The CW702 JPEG image-compression core derives from LSI Logic's L64702

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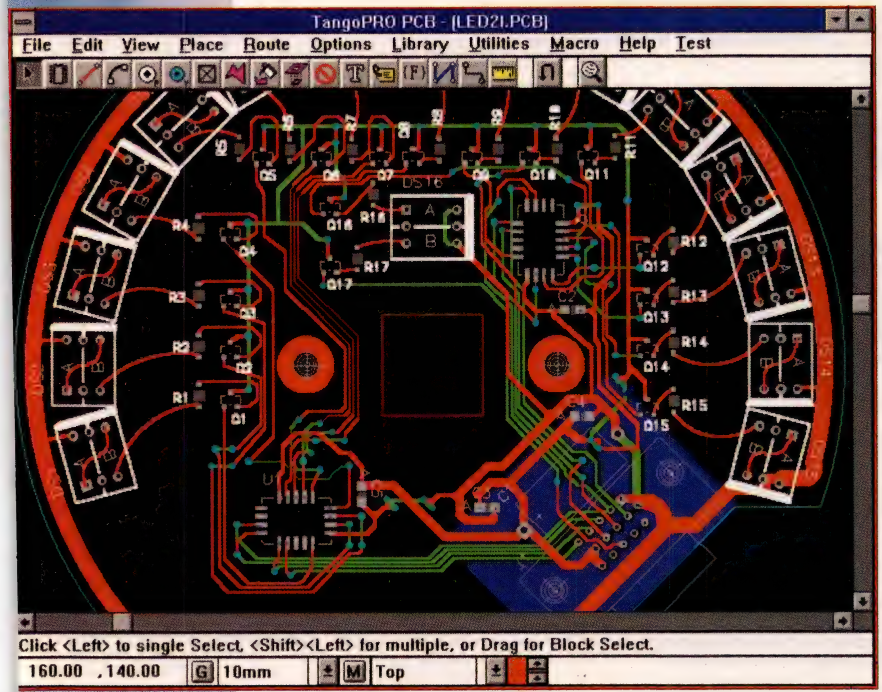

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Equation editor for Windows. Wiziword 3.0 is a WYSIWYG product that combines document processing, object-oriented drawing, plotting, equation editing, and both text and graphics filters. The equation editor is based on TeX, the markup language developed by Donald Knuth. The package is available for Windows, Macintosh computers, and most popular workstations. Windows version, $595; Macintosh version, $395; workstation versions, $695. **Microsystems Engineering Co,** 2500 W Higgins Rd, Suite 950, Hoffman Estates, IL 60195. Phone (708) 882-0111. Fax (708) 882-8397. **Circle No. 456**

Motion-picture file manager for OS/9, OS/9000. The Motion Picture File Manager (MPFM) runs on OS/9 and OS/9000 and allows real-time playback of MPEG-encoded audio and video files. MFPM is available with video drivers for the Motorola MCD250 and the C-Cube CL450 MPEG video decoders. It is also available with audio drivers for the Motorola MCD260 and the Analog Devices ADSP2105 DSP chips. The software is compliant with the ISO 11172 standard. $50,000. **Microware Systems Corp,** 1900 NW 114th St, Des Moines, IA 50325. Phone (800) 475-9000. Fax (515) 224-1352. **Circle No. 457**

CFI Design Representation toolkit. The Design Representation (DR) 1.0 Toolkit provides a set of basic tools to assist understanding and using Release 1.0 of the CAD Framework Initiative's (CFI) Design Representation Standard. That standard provides an information model and a programming interface that an EDA tool or design database can use to share netlist information with other DR 1.0-compliant tools and design databases. The toolkit provides tools for developing and testing both applications tools and design databases. It contains a copy of the DR standard, an example implementation of the Design Representation Programming Interface (DR-PI), data for an example circuit, tools

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COCOMO software cost-estimation tool. Costar, an interactive tool for estimating the cost of software development, is based on the Constructive Cost Model (COCOMO) defined by Dr Barry Boehm in *Software Engineering Economics*. It produces estimates of a project's duration, staffing, and cost, so you can make trade offs and experiment with "what if" analyses to produce a project plan. You can use the tool during your project's definition phase to get early estimates and then produce more accurate forecasts as you refine your knowledge of the system you're developing. Versions are available for PC and VAX. Single copy, $800; site license, $3500. **Softstar Systems,** 28 Ponemah Rd, Amherst, NH 03031. Phone (603) 672-0987. **Circle No. 449**

Signal-integrity tools. The Aztec tools analyze signal integrity for ICs, MCMs, and pc boards. Different tools calculate parameters, simulate waveforms, and model ground planes. They run under X11R4 and OpenWindows on Sun workstations, and they are available with or without a Spice file generator. Individual tools from $5000 to $15,000; package, $35,000. **Arizona Packaging Software Inc,** 1840 E River Rd, Suite 100, Tucson, AZ 85718. Phone (602) 577-8886. Fax (602) 577-0687. **Circle No. 450**

Visual programming tools for Windows, NT. New visual programming tools for Windows and Windows NT include the Visual C++ development system, the Delta version-control system, the Microsoft Developer Network (MSDN), and the Visual Control Pack. MSDN provides technical and strategic developer information; the Visual Control Pack is a collection of custom controls for the Visual C++ or the Visual Basic programming system. Visual C++, $199 (standard version) and $499 (professional version); Delta, $499; MSDN, $195 per year; Visual Control Pack, $199. **Microsoft Corp,** 1 Microsoft Way, Redmond, WA 98052. Phone (206) 882-8080. **Circle No. 451**

GUI tool and X-Base conversion tool. GUI Assist helps you develop graphical user interfaces for OS/2 application programs, taking advantage of Microsoft's Visual Basic and Windows. In most cases, you can create Windows-like presentations for DOS programs without rewriting any of the original code. Another tool, X2c, lets you recompile X-Base application programs to C for OS/2. GUI Assist, $125; X2c, $995. **TSLI Inc,** Executive Court One, 2295 Corporate Blvd NW, Boca Raton, FL 33431. Phone (407) 994-4466. Fax (407) 994-6304. **Circle No. 452**

Run-time error detection for C and C++. Purify 2, for use with C and C++ on Unix systems, eliminates run-time memory-access errors and memory leaks. It includes an incremental linker and, for remote error reporting, a mail mode. The tool's features shorten build times and thus speed code testing. $4000 per floating network license. **Pure Software Inc,** 1309 S Mary Ave, Sunnyvale, CA 94087. Phone (408) 720-1600. Fax (408) 720-9200. **Circle No. 453**

VHDL libraries for ASICs. Designers who use AT&T's 0.6- and 0.9-μP CMOS cell libraries, with 3V and 5V options, can now use Synopsys' VHDL System Simulator. The libraries have support for full timing and back-annotation, letting you specify and validate ASIC-based system designs and evaluate performance within the Synopsys design environment. The Synopsis simulator provides full support for IEEE-1076 VHDL. Price for library use depends on ASIC contract. **AT&T Microelectronics,** Dept AL-500404200, 555 Union Blvd, Allentown, PA 18103. Phone (800) 372-2447, ext 860; in Canada, (800) 553-2448, ext 860. Fax (215) 778-4106. **Circle No. 454**

Data-acquisition and -analysis software for Windows. Snap-Master 2.0 lets engineers and scientists acquire, display, analyze, and output data. It integrates sensors, transducers, and signal conditioning with a data-acquisition system. The new version includes support for Dynamic Data Exchange (DDE), zooming and panning for large files, multiple cursors, and event markers. $1985. **HEM Data Corp,** 17336 Twelve Mile Rd, Southfield, MI 48076. Phone (313) 559-5607. Fax (313) 559-8008. **Circle No. 455**

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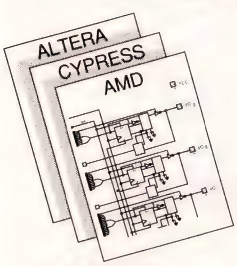

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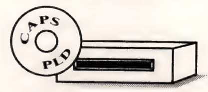

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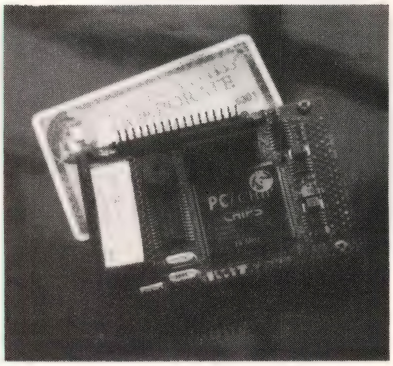
Test & Measurement Instruments

500M- to 2G-sample/sec DSOs. Four new DSOs replace older members of the vendor's 54500 series. The new units have real-time sampling rates that range from 500M to 2G samples/sec, bandwidths from 125 to 500 MHz, two or four channels, prices from $9500 to $21,000, and delivery times from 6 to 16 weeks, ARO. Each scope features a 1.44-Mbyte MS-DOS-compatible floppy-disk drive and 32k points of memory per channel. The scopes trigger on 1-nsec glitches and perform FFTs. All units offer a sequential single-shot mode that allows segmentation of their memories into multiple records, enabling the storage of multiple events, even those that occur in rapid succession. A time-tag feature stores each event's time of occurrence. To prevent aliasing, the two 2G-sample/sec-max scopes offer a peak-detect mode in which they *never* take fewer than 1G samples/sec. To avoid overrunning their memories, the scopes store only the highest and lowest values acquired during the display interval and plot a vertical line between them. **Hewlett-Packard Co,** Box 58059, MS 51L-SJ, Santa Clara, CA 95051. Phone (800) 452-4844. **Circle No. 441**



Credit-card-size data logger. The GCAT2000/3000 card pair, which is based on the CT F8680 80386-compatible CPU, can boot from MS-DOS in ROM and drive a 640×200-pixel LCD or CRT. Each card measures 2.6×3.4 in. The unit includes a 6-channel, 13-bit ADC with 10-µsec conversion time. A FIFO memory stores series of ADC readings. Also included are floppy- and hard-disk controllers, a parallel port, two serial ports, a mouse port, a slot compatible with the Personal Computer Memory Card International Association standard, a clock calendar, a negative-voltage generator for LCDs, 1 Mbyte of DRAM, and 512 kbytes of ROM. $799. **Saelig Co,** 1193 Moseley Rd, Victor, NY 14564. Phone (716) 425-3753. Fax (716) 425-3835. **Circle No. 442**

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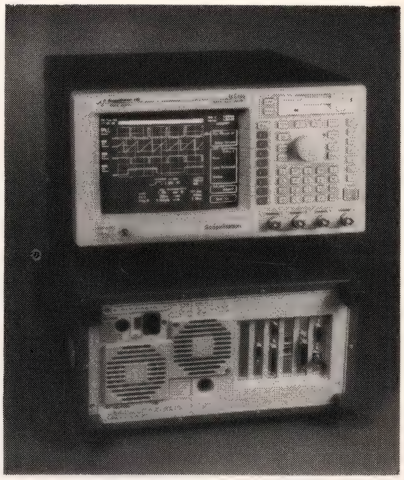
60- to 200-MHz, 2- and 4-channel analog scopes. The TAS 400 series now includes true 4-channel units with 100- and 200-MHz bandwidth, in addition to the 2-channel 60- and 100-MHz units introduced last year. The new models (100-MHz, $2395; 200-MHz, $3495) offer user interfaces similar to those of the vendor's TDS series of DSOs. This similarity allows someone familiar with one series to immediately use scopes from the other. Although some competitive 4-channel scopes include only limited attenuators on two channels (so-called 2+2 models), these 4-channel units provide full attenuators on all channels. **Tektronix Inc,** Box 1520, Pittsfield, MA 01202. Phone (800) 426-2200. **Circle No. 443**

Remote data-acquisition system. Each DVT Series 50 unit has eight digital I/O lines and eight analog inputs. Each unit includes an RS-232C port, a printer port, and a modem. The intelligent modules can perform autocalibration, check inputs against limits, and provide alarm outputs. From less than $500. **Dancer Communications Inc,** 114 Walnut St, Morton, PA 19070. Phone (215) 543-8066. Fax (215) 543-2151. **Circle No. 444**

Dual-channel frequency synthesizers. The PTS 620 provides two independent 1- to 620-MHz synthesizers in a single 5¼-in.-high, rack-mountable enclosure. The units, which you program by supplying parallel TTL, binary-coded-decimal inputs, provide 0.1-Hz resolution from 1 to 310 MHz and 0.2-Hz resolution above. In the decades from 100 kHz to 0.1 Hz, switching is phase continuous. The oven-controlled frequency standard is stable to 3 ppb/day and 1 ppm/year. $12,725; delivery, 60 days, ARO. **Programmed Test Sources Inc,** Box 517, Littleton, MA 01460. Phone (508) 486-3008. Fax (508) 486-4495. **Circle No. 445**

4-GHz-timing/1-GHz-state logic-analysis modules. The 16515A, 16516A, 16517A, and 16518A are plug-in cards for the 16500A and B logic-analyzer mainframes. On eight channels per card, the plug-ins do timing analysis at 4G sample/sec and state analysis at 1G sample/sec. A mainframe accepts five cards, and you can add one expansion unit that accepts five more. Cutting the sampling rate in half doubles the number of channels per card. The master plug-in for state and timing analysis costs $13,500; the slaves cost $13,000 each. The master plug-in for timing analysis only costs $9185; slaves cost $8160 each. Delivery is 16 to 20 weeks, ARO. **Hewlett-Packard Co,** Box 58059, MS 51L-SJ, Santa Clara, CA 95051. Phone (800) 452-4844. **Circle No. 446**



DSO with advanced communication capabilities. The ScopeStation 140, a 100-MHz-bandwidth, 200M-sample/sec scope, can send faxes of waveforms. The 4-channel DSO features direct connection to Ethernet networks. To prevent aliasing, the scope—which includes a 3½-in. floppy-disk drive as well as RS-232C and Centronics ports—always digitizes at full speed. At lower sweep speeds, to avoid overrunning its 2k-sample per channel memory, it stores only the maximum and minimum values in each sampling interval and connects them on the screen with a solid vertical line. Less than $5000. **LeCroy Corp,** 700 Chestnut Ridge Rd, Chestnut Ridge, NY 10977. Phone (914) 578-6035. Fax (914) 425-8967. **Circle No. 447**

Programmer for PIC16C71 18-pin µP. The $144.95 Picquick programmer, which connects to the parallel port of an MS-DOS PC, programs both the EPROM and one-time-programmable versions of the low-cost microcontroller. The programming algorithm is the one suggested by the IC manufacturer. **Eltronics Ltd,** 704-33 Orchardview Blvd, Toronto, Ont Canada M4R 2E9. Phone (416) 483-7678. Fax (416) 483-2406. **Circle No. 448**

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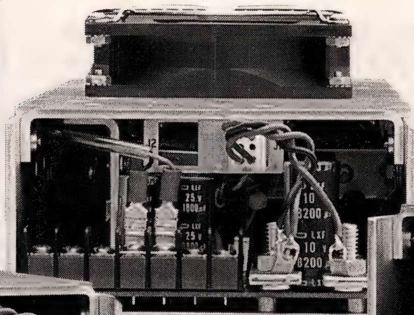

OFSX 800 SF
800 Watts
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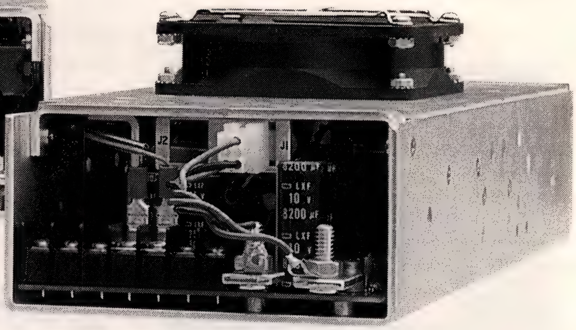
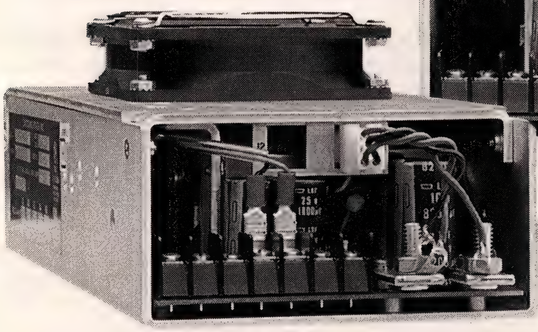
12 VDC @ 10 Amps
24 VDC @ 5 Amps



OFSX 300 SF
300 Watts
5" wide x 2.6" high x 8.5" long

5 VDC @ 40 Amps
12 VDC @ 10 Amps
12 VDC @ 3 Amps



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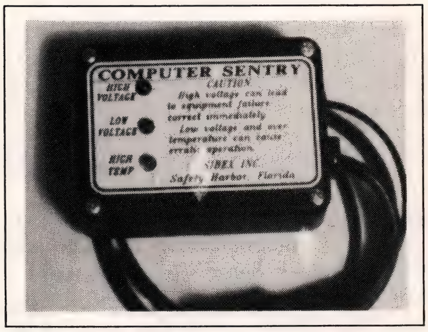


enclosure and does not require you to open the PC for installation. It connects in-line with the keyboard cable; a small temperature probe extends into the PC through any opening on the rear of the PC. $49.95. **Sibex Inc,** 1040 Harbor Lake Dr, Safety Harbor, FL 34695. Phone (813) 726-4343. **Circle No. 476**

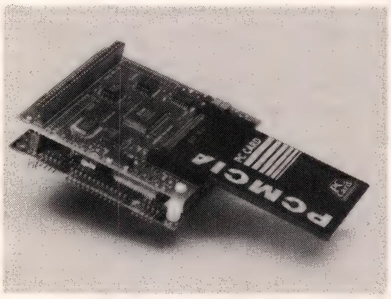
Rack-card short-range modem. Model 1080RC 2U rack-card short-range modem provides RS-232C data rates to 19.2 kbps over one or two unconditioned twisted pairs. The modem works with both software (X-On/X-Off) and hardware (RTS/CTS) handshaking and has built-in V.54 loopback test and V.52 bit-error-rate test. Transmissions as far as 10 mi are possible over #24 AWG twisted-pair wire. $279. **Patton Electronics Co,** 7958 Cessna Ave, Gaithersburg, MD 20879. Phone (301) 975-1000. Fax (301) 869-9293. **Circle No. 477**

VME SCIM expansion board. The VSIP 6U slave VME board accepts as many as four standard or custom modules that comply with specifications of the Standard Computer Interface Module (SCIM) bus. Modules for the open-architecture SCIM mezzanine bus provide analog and digital I/O, memory, graphics, and communications functions. Use of the modules reduces the board count of most VMEbus systems by at least one. $450; SCIM modules, from $120. **Arcom Control Systems Inc,** 13510 S Oak St, Kansas City, MO 64145. **Circle No. 478**

Image-processing modules. The TIM-40 CFG frame grabber and the TIM-40 CD color-display boards adhere to the TIM-40 industry standard. The boards allow data transfers at 20 Mbytes/sec to other TIM-40 modules for distributed image processing. The products support the 3L Parallel C compiler and the Helios operating system. Each board uses a TMS320C40 parallel DSP chip. CFG, £4000; CD, £4500. **NEL,** East Kilbride, Glasgow G75 0QU, Scotland. Phone (44)(41) 607-272-4417. Fax (44)(41) 607-277-2200. **Circle No. 479**

Industrial computer with SVGA. The Model 8540-RV rack-mount industrial computer includes a 14-in. Super VGA monitor with a 13-in. diagonal viewing area. The unit's front panel conforms to NEMA specifications; a lockable door on the panel conceals controls and connectors for security. The unit measures 19 × 12.22 × 24 in. and includes a 250W power supply. $3995. **Industrial Computer Source,** 10180 Scripps Ranch Blvd, San Diego, CA 92131. Phone (619) 271-9340. Fax (619) 271-9666. **Circle No. 480**

Computers & Peripherals



PC/104-based PCMCIA card drive. Card Drive P104, which operates in PC/104 embedded systems, reads and writes PCMCIA (Version 2.0) and JEIDA cards. It supports both I/O cards, such as fax/modems and LAN cards, and memory cards. Supported memory cards include SRAM and flash cards; flash technology support includes devices from AMD, Intel (Series 1 and Series 2), and Sundisk. The card drive stacks in a PC/104 configuration. The complete package includes the drive, device drivers, utility programs, and documentation. $275 (1 to 9 units). **Adtron Corp**, 3050 S Country Club Dr, Suite 24, Mesa, AZ 85210. Phone (602) 926-9324. Fax (602) 926-9359.
Circle No. 467

Self-refreshed DRAM cards. Four new 88-pin JEIDA/JEDEC DRAM cards contain their own refresh circuitry, allowing you to shut down all system-refresh circuitry, including μPs. Two cards hold 2 Mbytes of data (512k × 32 and 512k × 36 bits); two other versions hold 4 Mbytes (1M × 32 and 1M × 36). The cards require a single 5V supply and are available with access times of 70 and 80 nsec. The 80-nsec, 4-Mbyte card, $240 (100). **Hitachi America Ltd,** 2000 Sierra Point Pkwy, MS-080, Brisbane, CA 94005. Phone (800) 285-1601, ext 16; (415) 589-8300. Fax (415) 583-4207. Request literature package M16P009. **Circle No. 468**

Flat-panel terminal. The INX5000T flat-panel display terminal provides monochrome VGA-compatible graphics on an 11.3-in. screen. It accepts either RS-232C or RS-485 input and includes ANSI 3.64 and VT100 terminal emulation. The unit is less than 2 in. deep and has a NEMA 4/12 front panel and a sealed 40-position membrane keypad. $1295. **Ann Arbor Technologies Corp,** Box 3083, Ann Arbor, MI 48106. Phone (313) 995-1360. Fax (313) 662-3707.
Circle No. 469

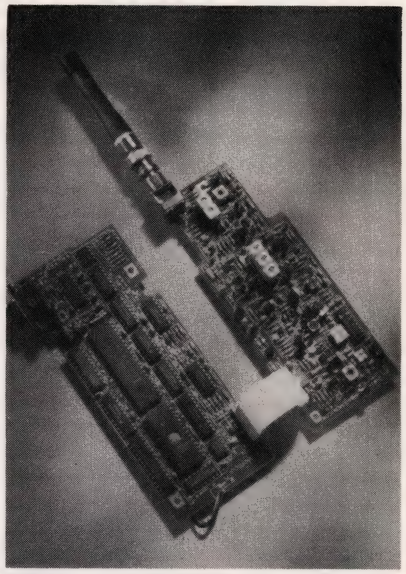
JPEG evaluation board. The JView board, designed around the manufacturer's JPEG processor IC, allows you to evaluate that chip and JPEG software-development tools. The PC/AT ISA card demonstrates multimedia functions for still images and live video. It records images to a hard disk and plays them back to a video window overlaid on standard VGA. Supplied software demonstrates full-motion video compression and decompression. $3900, including application software. **LSI Logic Corp,** 1551 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 433-8000. **Circle No. 470**

PC-to-mainframe adapter. The IRMA Pocket 3270 adapter connects portable and desktop PCs to mainframe 3270 computers. The device connects to a PC's parallel port and a 3270 controller via coaxial or twisted-pair cable. It comes with a power supply and software. $695. **Digital Communications Associates Inc,** 1000 Alderman Dr, Alpharetta, GA 30202. Phone (800) 348-3221. Fax (404) 442-4364. **Circle No. 471**

Printer servers. Two Pocket Print Servers, models ESI-2848A and ESI-2831A, allow parallel-port printers to connect to Token Ring and TCP/IP Ethernet networks, respectively. Printers connect directly to the networks; chaining a printer to a file server or a workstation isn't necessary. The products use flash memory to store network software, so software upgrades will be easy. ESI-2848A, $795; ESI-2831A, $495. **Extended Systems,** 5777 N Meeker Ave, Boise, ID 83704. Phone (800) 235-7576; (406) 587-7575. Fax (208) 377-1906. In Europe, phone (49) 7034-27326. Fax (49) 7034-27364.
Circle No. 472

VME RISC board. The 38-10A VMEbus computer board includes a 40-MHz R3000 RISC processor, Ethernet and SCSI-2 interfaces, four serial ports, and as much as 16 Mbytes of DRAM. The RISC processor is an IDT 3081E μP, which includes an R3010 floating-point accelerator and 20 kbytes of configurable on-chip instruction- and data-cache memory. Board memory is a 32-bit-wide, interleaved DRAM array that is closely coupled with the processor. $4495. Delivery, eight weeks ARO. **Radstone Technology,** 20 Craig Rd, Montvale, NJ 07645. Phone (800) 368-2738. **Fax (201) 391-2899.** **Circle No. 473**

VME SCSI module. The CXM-SCSI extends the control, address, and data lines of a VME board's μP and provides a SCSI connection on a VMEbus mezzanine. The module conforms to the public-domain Controller eXtension Connector specification. With its 3U form factor, it's about one-third the size of a full-height VME board. $290. **PEP Modular Computers,** 750 Holiday Dr, Bldg 9, Pittsburgh, PA 15220. Phone (800) 228-1737; (412) 921-3322. Fax (412) 921-3356. **Circle No. 474**



Radio-modem board set. The System 200 radio-modem board set for PCs communicates RS-232C data via FM signals between 450 and 470 MHz. One board is a transceiver, and the other is a modem. The base-station antenna is a quarter-wave whip; peripheral nodes use a heliflex. Transmission levels range from 1 mW to 2W; at 2W, line-of-sight connectivity is 2 mi or more. $465 (1000). Delivery, 90 days ARO. **Monicor Electronic Corp,** 2964 NW 60th St, Fort Lauderdale, FL 33309. Phone (305) 979-1907. Fax (305) 979-2611.
Circle No. 475

PC-condition monitor. Computer Sentry monitors voltages and temperature in a PC and warns against harmful conditions. The module mounts on the PC

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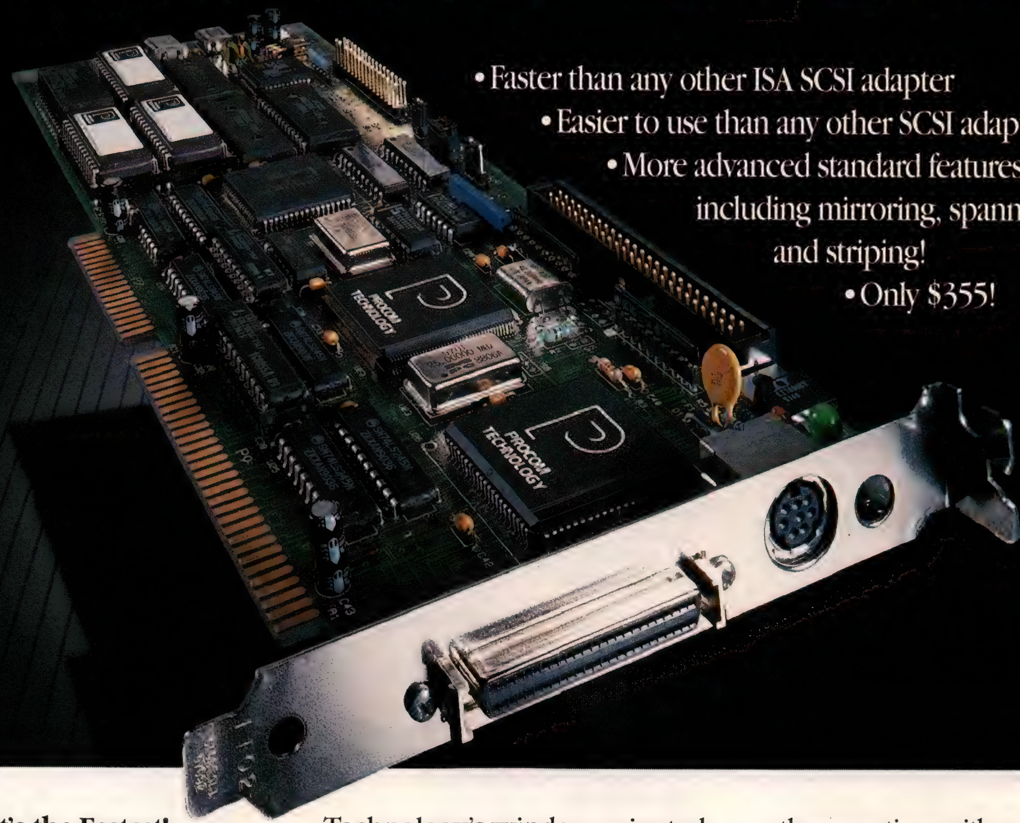

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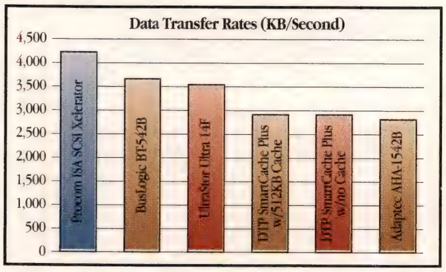

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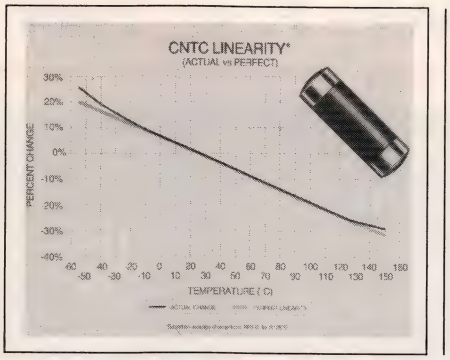
CIRCLE NO. 32

connectors, or automatic-bus-grant connectors. $1095 for a 21-slot unit with standard DIN connectors. **Hybricon Corp,** 12 Willow Rd, Ayer, MA 01432. Phone (508) 772-5422. Fax (508) 772-2963. **Circle No. 435**

Thermistors. The CNTC1/8 features a 1% max linearity deviation over a −10 to +130°C range. The cylindrical thick-film device is rated for 400 mW at 25°C and is available in resistance values of



500Ω to 10 kΩ. Resistance tolerance equals 2%; the negative temperature coefficient of resistance measures −2500 ppm/°C. The unit fits an industry-standard 1206 footprint for surface-mount applications. From $0.65 (1000). **IRC Inc,** 305 Greenway Rd, Boone, NC 28607. Phone (704) 264-8861. Fax (704) 264-8865. **Circle No. 436**

Small-signal transistors. The LT4217A and LT4239A small-signal transistors feature typical cutoff frequencies of 6 GHz, gain of 19 dB at 300 MHz, 2-dB noise figures at 300 MHz, and a maximum current rating of 400 mA. The 4217A is housed in a 0.28-in. stud package; the 4239A is housed in a conventional TO-39 package. LT4217A, $7.30; LT4239A, $2.70. **Motorola Inc,** 5005 E McDowell Rd, Phoenix, AZ 85008. Phone (602) 244-3818. Fax (602) 244-4597. **Circle No. 437**

Futurebus+ backplanes. These Futurebus+ backplanes have an 8-layer design. The 14-slot units suit applications that involve 128 data bits, 64 address bits, and 80 I/O pins per slot. Features include a 52Ω impedance, active terminations, and 224A bus bars for 5V, 3.3V, and ground. From $3000. **Electronic Solutions,** 6790 Flanders Dr, San Diego, CA 92121. Phone (800) 854-7086; (619) 452-9333. Fax (619) 452-9464. **Circle No. 438**

Keyswitches. ML Series keyswitches feature a full 3-mm travel and have a rated life of 10 million actuations min. The devices are supplied ready for pc-board mounting and require no special tooling. The single-pole NO units are rated for 12V and 10 mA max. Contact force measures 0.353 to 1.2324 oz. **Cherry Electrical Products,** 3600 Sunset Ave, Waukegan, IL 60087. Phone (708) 360-3599. **Circle No. 439**

Touch screen. The Quikpoint GX140 is a plug-and-play touch screen that snaps onto the front of any 13- or 14-in. monitor. The unit's controller card easily installs on the PC bus or it can reside in a stand-alone chassis that connects to the computer's serial port. The system has a 1024×1024 touch-point resolution and records a touch within 15 msec of finger contact. $695. **Microtouch Systems Inc,** 55 Jonspin Rd, Wilmington, MA 01887. Phone (508) 694-9900. FAX (508) 694-9980. **Circle No. 440**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The MJTP1230 through-hole version, $0.094 (10,000). **MORS/ASC,** 134 Water St, Wakefield, MA 01880. Phone (617) 246-1007. Fax (617) 245-4531.
Circle No. 430

DC/DC converters. Series 1600 16W converters are available in 1-, 2-, and 3-output versions. All are approved to the latest revisions of UL 1950 and CSA 22.2. The 24 models in the series operate from 9 to 72V and output combinations of 5, 12, 15, ±5, ±12, or ±15V. I/O isolation equals 500V dc, and output accuracy measures ±1%. All models include remote on-off control inputs and an input pi filter to reduce reflected ripple current. $73.50 to $87.50 (100). **Conversion Devices Inc,** 15 Jonathan Dr, Brockton, MA 02401. Phone (508) 559-0880. Fax (508) 559-9288. **Circle No. 431**

Rocker switches. Series 8090 switches snap into 22×30-mm panel cutouts. The units are rated for 16A at 125V ac, 10A at 250V ac, and 16A at 28V dc. The devices are available in spst and dpst versions. The switches are UL recognized, CSA certified, and VDE approved. $0.91 (1000). Delivery, 8 to 10 weeks ARO. **Eaton Corp,** 4201 N 27th St, Milwaukee, WI 53216. Phone (414) 449-7483. **Circle No. 432**

Coaxial attenuators. LAV Series continuously variable coaxial attenuators span the dc to 800-MHz range and feature 0-to 20-dB attenuation. The units are available in 50 and 75Ω versions. AV Series units are designed for narrow, octave, or multioctave service over the 0.95- to 26-GHz range. They feature 0-to 35-dB attenuation, 0.3-dB insertion loss, 1.3:1 VSWR, and 5W power ratings. From $125. Delivery, stock to eight weeks ARO. **RLC Electronics Inc,** 83 Radio Circle, Mount Kisco, NY 10549. Phone (914) 241-1334. Fax (914) 241-1753. **Circle No. 433**

External power supplies. TPES20, TPES40, and TPES60 Series universal-input supplies include 36 models with single, dual, and triple outputs. Power ratings range to 60W. All models have 2% load and 0.2% cross regulation on the main output. Cases have impact-resistant thermoplastic, which carries a 94V-1 UL rating and a 94V-0 CSA rating. Operating range spans 0 to 40°C. $70 (100). Delivery, 8 to 10 weeks ARO. **Total Power International Inc,** 418 Bridge St, Lowell, MA 01850. Phone (508) 453-7272. Fax (508) 453-7395.
Circle No. 434

VME-system backplanes. HP Series 10-layer backplanes are designed for VME systems. Available in versions with 3 to 21 slots, the units feature a stripline construction. The units have in-board terminations, shrouds on all connectors, and several power options. The backplanes come with standard 3-row DIN connectors, enhanced DIN

Components & Power Supplies

Voltage dividers. These 3-terminal dividers are available in gigohm values with ratios in the thousands and tolerances to 1%. Other specifications include a 10-ppm/°C temperature coefficient of resistance tracking, 0.1-ppm/°C voltage linearity, and 30,000V working voltage rating. Standard units are available in 100- and 1000-MΩ values. $5.75 (100). **Ohmcraft,** 3800 Monroe Ave, Pittsford, NY 14534. Phone (716) 586-0823. Fax (716) 586-0015. **Circle No. 420**

DC/DC converter. The MHF+2805D converter outputs 15W from a 1.12×1.45×0.33-in. case—a 30W/in.^{3} power density. The units develop a ±5V output from a 28V input. Line and load regulation equals 15 mV typ, and

input ripple is 25 mA p-p. Audio rejection equals 50 dB; efficiency ranges to 82%. Operating range spans −55 to +125°C. From $353 (100). Delivery, eight weeks ARO. **Interpoint Corp,** Box 97005, Redmond, WA 98073. Phone (206) 882-3100. Fax (206) 882-1990. **Circle No. 421**

Lightning suppressors. The Model 29 single-stage DB-9 lightning suppressor comes in two versions: The 29 accommodates RS-232C levels, and the 29-1 works with RS-422 levels. The unit installs between the serial data cable and the DB-9 data port on a 386- or 486-based PC, laptop, or similar device. The unit employs avalanche diodes as suppression devices. Reaction time equals 2 nsec max. The 29-1 also accommodates EIA-530 interfaces and MIL-STD-188-114. $44. **Telebyte Technology Inc,** 270 E Pulaski Rd, Greenlawn, NY 11740. Phone (800) 835-3298; (516) 423-3232. Fax (516) 385-8184. **Circle No. 422**

DIN connectors. These 2-part connectors meet DIN 41612, VG 95324, and IEC 130/14 standards. The line includes a 48-position Form F unit rated for 4A that comes with or without polarization keys; 11- and 15-position Form H15

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units rated for 15A; Form H15 devices with 7 or 10 contacts rated for 15A and 2 or 4 contacts rated at 50A; and mixed versions. $3 to $30. **Bicc-Vero Electronics Inc,** 1000 Sherman Ave, Hamden, CT 06514. Phone (800) 242-2863. Fax (203) 287-0062. **Circle No. 423**

Surge suppressors. These devices can withstand a 24.5V jump-start for five minutes. The line includes three units—the 3J V18AUMLA1210, the 10J V18AUMLA1812, and the 25J V18A-UMLA 2220. All units have an 18V rating. V18AUMLA1210, $0.41; V18A-UMLA1812, $0.70; V18AUMLA2220, $1.15 (1000). **Harris Semiconductor,** Box 883, Melbourne, FL 32901. Phone (800) 442-7747. **Circle No. 424**

Coaxial switches. These failsafe coaxial switches are available in two lines: SS Series units, which operate over a dc to 18-GHz range, and HS Series devices, which have a dc to 12.4-GHz operating range. The spdt units switch in 20 msec. The SS units are available with SMA connectors. From $215. **Alan Industries Inc,** 745 Greenway Dr, Columbus, IN 47202. Phone (800) 423-5190. Fax (812) 372-5909. **Circle No. 425**

DC/DC converters. DC2-40 40W dual-output, open-frame converters operate from 36 to 72V inputs. The four models in the line output combinations of 5 and 12, 15, 24, or 25V. Key features include soft start, current limiting, short-circuit/overvoltage protection, and 3000V I/O isolation. The units include EMI/RFI suppression filters. $40 (OEM qty). **Nidec/Power General,** 152 Will Dr, Canton, MA 02021. Phone (617) 828-6216. Fax (617) 828-3215. **Circle No. 426**

LED pc-board mount. The PCH 175 right-angle mount accommodates both bilead and trilead LEDs. The mount forms the bileads to meet conventional 0.1-in. pad spacings and forms the trileads in a triangular pattern, which staggers the leads for easier pc-board insertion. Its housing material carries a 94V-0 UL rating. $0.04 (10,000). **Visual Communications Co Inc,** 7920-G Arjons Dr, San Diego, CA 92126. Phone (619) 549-6900. **Circle No. 427**

Trimmers. G4S trimmer potentiometers are side-adjust, surface-mountable devices. Resistance values range from 10Ω to 2 MΩ, and tolerance equals ±20%. The 5×5.7×4.55-mm units are available in two versions: The A version has J-hook leads, and the B version has gull-wing terminals. Power rating equals 250 mW; operating range spans −55 to +125°C. The sealed devices are designed to accommodate flow and reflow soldering processes. $1.06 (1000). Delivery, six to eight weeks ARO. **Tocos America,** 565 W Golf Rd, Arlington Heights, IL 60005. Phone (708) 364-7277. Fax (708) 364-7317. **Circle No. 428**

Linear power supply. The Model 1.10.750's 10V output is suitable for driving transducer bridges. The 350-mA output can excite as many as 12 350Ω bridges. Line and load regulation equals ±0.1%, and noise and ripple figures measure 1 mV rms. Operating range spans −25 to +50°C. Versions operate from either 115 or 230V ac inputs. Foldback current limiting allows the units to be shorted indefinitely without damage. $110. **Calex Mfg Co Inc,** 2401 Stanwell Dr, Concord, CA 94520. Phone (800) 542-3355. Fax (510) 687-3333. **Circle No. 429**

Miniature switches. Series MJTP snap-dome miniature switches are available in through-hole and surface-mount versions. The single-pole, momentary-action units have contacts rated for 12V dc at 50 mA. Life is rated at 50,000 to 100,000 cycles. Various body styles have red, yellow, or green LEDs. The surface-mount units are compatible with most pick-and-place equipment.

ceive side. The chips are pin-compatible with Crystal Semiconductor's CS61535A and CS61574A devices. Applications include DSX-1 cross-connect switches, line interfaces for PCM multiplexers, digital switches, data service units, and channel service units. $9.70 (10,000). **VLSI Technology Inc,** 8375 S River Pkwy, Tempe, AZ 85284. Phone (602) 752-8574. Fax (602) 752-6000. **Circle No. 415**

10-bit RAM-DACs. Combining three 10-bit video RAM-DACs and a color-palette RAM in one package, ADV7150 family chips can simultaneously display 16.7 million colors. Features of the 170-MHz devices include 24-bit true color and 30-bit gamma-corrected operation. $83 to $148 (1000). **Analog Devices Inc,** 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1428. Fax (617) 821-4273. **Circle No. 416**

FPGA. The QL8x12A is a faster and less-expensive version of the QL8x12 FPGA. The 1000-gate device reduces the internal logic-cell delay from 3.4 to 2.4 nsec; an optimized layout reduces the die size by 20%. A dedicated clock network has a clock skew of 500 psec across the chip. The FPGA is available in a 100-pin, 1.4-mm-high quad flatpack for use in PCMCIA cards. The QL8-12A-2PL68C costs $37.60 (1000). **Quicklogic Corp,** 2933 Bunker Hill Lane, Santa Clara, CA 95054. Phone (408) 987-2000. FAX (408) 987-2012. **Circle No. 417**

SCSI bus terminator. The TL2218-285 active SCSI-bus current-mode terminator is compatible with the 27 channels of the proposed Fast SCSI III standard. The device terminates nine SCSI lines. The terminator is also compatible with active negation drivers, which are often used in high-speed SCSI systems. Besides operating in wide and fast SCSI III systems, the device can be used for single-ended active SCSI terminations. The output capacitance is 6 pF. $1.75 (1000). **Texas Instruments Inc,** Semiconductor Group, Literature Response Center, Box 17222, Denver, CO 80217. Phone (800) 477-8924, ext 3437. **Circle No. 418**

Multichip modules. The MMS-D300 series multichip modules come in small form factors. The modules operate at 10 MHz to 1 GHz. Features include die attachment using wirebond process, silicon-to-package area ratios of 40% to 80%, and a direct thermal path from silicon to a heat sink. Packaging options include QFPs, PLCCs, and thin QFPs conforming to JEDEC standards. Packages are as thin as 1.2 mm. Typical modules house between 2 and 10 CMOS ICs in die form. $10 to $50 (10,000). **Micromodule Systems Inc,** 10500 Ridgeview Ct, Cupertino, CA 95014. Phone (408) 864-7437. **Circle No. 419**

Switching regulators. The LTC1148 and LTC1149 step-down switching regulators have typical efficiencies of 95% when operating at no load current and a 200-μA supply current. The LTC1148 operates from input voltages of 4 to 16V; the LTC1149 operates from input voltages up to 48V. Both devices feature burst-mode switching, during which the chips switch external complimentary power MOSFETs at up to 250 kHz. Both devices also have short-circuit protection. LTC1148 in 14-lead SOIC, $4.25; LTC1149, $5.20 (100). **Linear Technology Corp,** 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-1900. Fax (408) 434-0507. **Circle No. 411**

ISA bus controller. The VL82C481 single-chip ISA bus controller has write-back control logic for 486-based systems. The chip fits into Intel's Overdrive Ready upgrade strategy. The chip's memory controller addresses 64 Mbytes of system memory, which can be 256-kbit or 1- or 4-Mbit DRAMs. The memory controller provides page-mode DRAM access and burst reads and writes. The direct-mapped write-back cache-control logic runs with 32 kbytes to 1 Mbyte of cache RAM. Power-on reset is optional. $22 (10,000). **VLSI Technology Inquiries,** 200 Parkside Dr, San Fernando, CA 91340. Phone (602) 752-6202. **Circle No. 412**

Graphics accelerator. The TGUI9420 graphics accelerator has both VL and ISA bus interfaces. The accelerator

linearly addresses 2 Mbytes of DRAM. The chip operates with 256k × 4-, 512k × 8-, or 256k × 16-bit DRAMs. The operations the graphics engine performs include pixel bit block transfer (bitblt), line draw, short-stroke vector draw, area fill, and image transfer. Extended graphics modes include 640 × 480 pixels with 32k, 64k, or 16.8M colors and 1024 × 768 pixels with 256 colors. $31.50 (1000). **Trident Microsystems Inc,** 205 Ravendale Dr, Mountain View, CA 94043. Phone (415) 691-9211. Fax (415) 691-9260. **Circle No. 413**

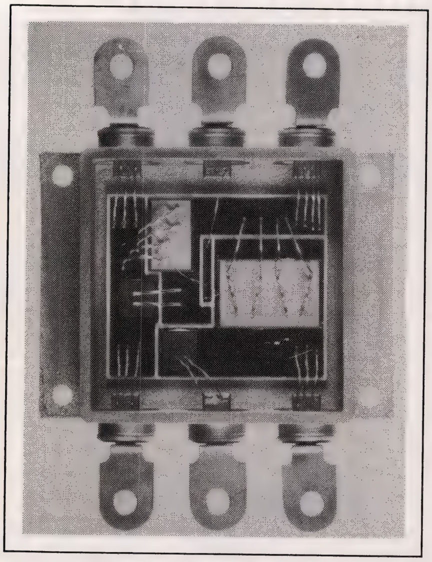
Analog switches. Three CMOS analog switches have a maximum on-resistance of 35Ω. The DG417 is a SPST normally open (NO) switch, the DG418 is a SPST normally closed (NC) switch, and the DG419 is a SPDT NO/NC switch. The devices have a breakdown voltage of 44V, a maximum turn-on time of 175 nsec, and a maximum turn-off time of 145 nsec. DG417 and DG418, from $1.19; DG419, from $1.63 (1000). **Maxim Integrated Products,** 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600, ext 6087. **Circle No. 414**

T1/E1 line-interface units. The VP14335 and VP14574 chips can synthesize DSX-1 and CCITT G.703 pulses. The VP14335 provides jitter attenuation on the transmit side; the VP14574 provides jitter attenuation on the re-

Integrated Circuits

Full-duplex Ethernet controllers. The 80C04 chip set has a full-duplex switching hub that lets 10Base-T nodes simultaneously transmit and receive data. Full-duplex data transfer effectively doubles the network bandwidth to 20 Mbps. The packet delay, which equals the central-switch delay, is predictable. The chip set employs a 33-MHz bus clock and has byte-swap control. It also has address and hash filters for sorting multicast addresses. $13 (10,000). **SEEQ Technology Inc,** 47131 Bayside Pkwy, Fremont, CA 94538. Phone (510) 226-7400. Fax (510) 657-2837. **Circle No. 401**

Programmable filter/equalizer. The ML6017 filter/equalizer suits products having variable-speed data streams. You can tune the chip to track data streams of 9 to 48 MHz. A serial interface programs the chip on the fly. The chip contains two programmable filters: a lowpass filter, which removes high-frequency noise, and a bandpass filter, which removes low-frequency noise and high-frequency overtones. A programmable equalizer overcomes intersymbol interference. In a 20-pin super-small-outline package, $5.95 (100,000). **Micro Linear Corp,** 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 433-5200. **Circle No. 402**



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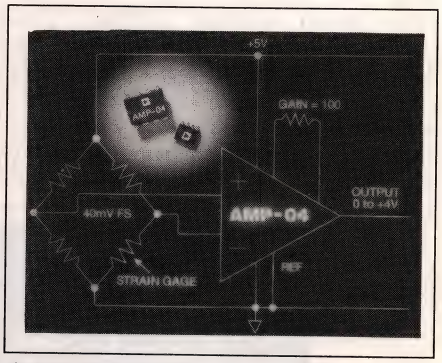

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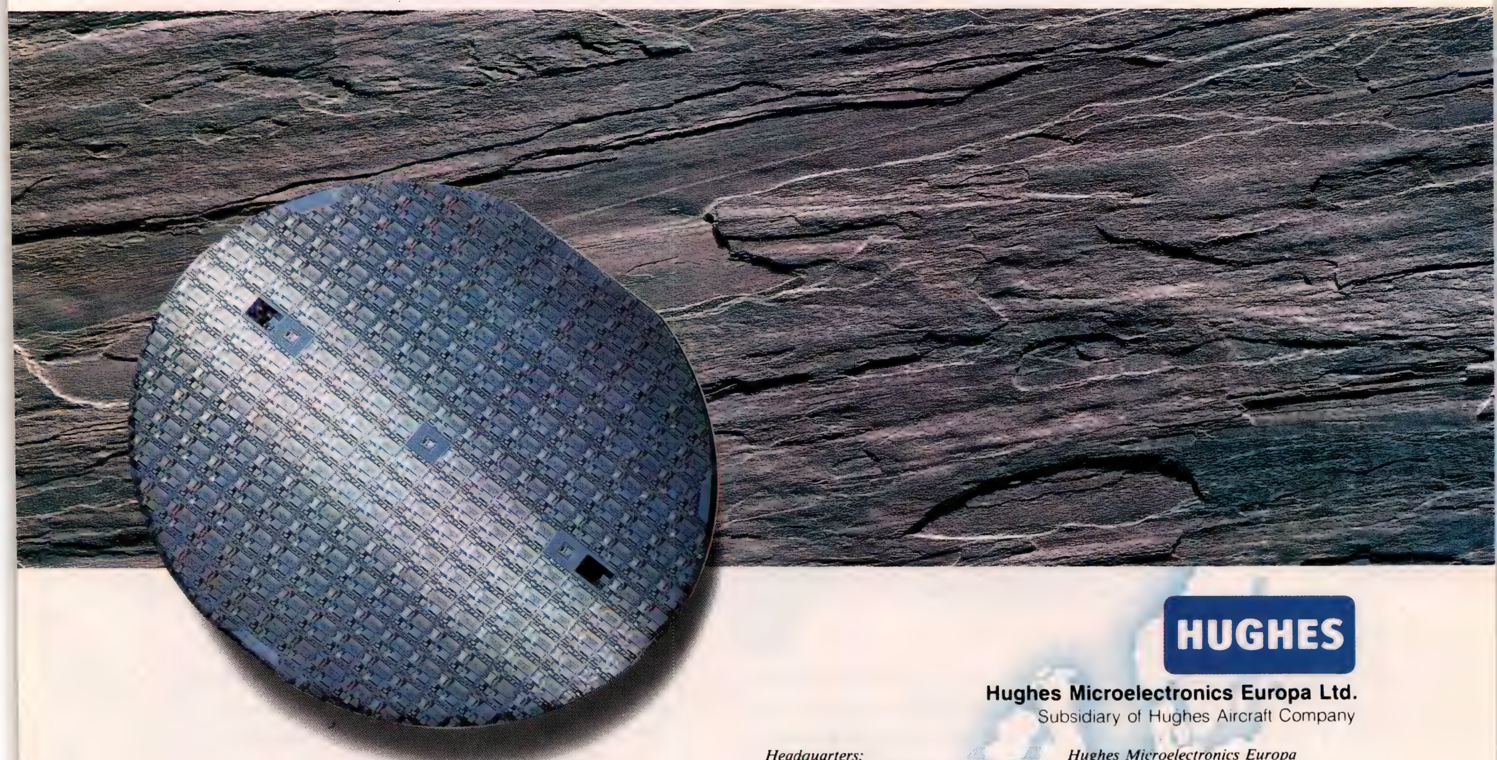

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ISSUE WINNER

The winning Design Idea for the October 1, 1992, issue is entitled "Differential amplifier reduces parts count," submitted by Irwin Cohen of Hewlett-Packard (Waltham, MA).

The winning Design Idea for the October 15, 1992, issue is entitled "1.5 to 5V converter supplies 200 mA," submitted by Jim Williams of Linear Technology Corp (Milpitas, CA).

Reset trap locates system errors

Ed Thompson, Micro Computer Control, Hopewell, NJ

Unexpected system resets during development can often lead to much finger pointing between hardware and software team members. A simple technique can isolate the problem to either hardware or software, reduce frustrations, and speed debugging. The technique relies on the fact that a hardware reset sets processor registers to a known initial state, and software then initializes those same registers to another state. By testing the state of a register before software initialization, you can detect the cause of the reset. The solution presented here is for an 8051-based system, but could easily be adapted to a variety of system architectures.

Listing 1—Startup code to trap reset cause

```
#define TMOD 0x03 /* Timer0 = 16-bit */

bit sw_reset;      /* TRUE on Software Reset */

main()
     {
     sw_reset = (tmod == TMOD); /* Test Reset */
     .
     tmod = TMOD; /* Software Initialization */
     .
     .
     }
```

Listing 1 shows a sample section of C code to handle startup and initialization of the 8051 TMOD register. A hardware reset initializes this register to zero (00H). The code tests the state of this register against the software initialized value, and records the test result for later examination. You can write additional code to send this result to a spare I/O pin or output it to the UART upon receiving an appropriate inquiry. It's worthwhile to leave this code as a permanent part of the system to help explain unexpected reset events that could occur at later stages of system development and testing. **EDN BBS /DI_SIG #1213** EDN

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CIRCLE NO. 29

and the cycle repeats itself, operating again in the strobe mode unless the load current drops below 1A. With the component values in the figure, pulse ON is about 200 µsec with 0.5 sec between pulses.

You can separate the V_{CC} of the LM10 and the load. The V_{CC} for the LM10 must stay within the gate threshold voltage and the V_{GS} rating of Q_1. The V_{CC} for the load must be lower than the $V_{BR(DSS)}$ of Q_1. **EDN BBS /DI_SIG #1238**

To Vote For This Design, Circle No. 393

Address latch increases µP's data width

Shwang-Shi Bai, Chung-Shan Institute of Science and Technology, Lung-Tan, Taiwan

Many 8-bit µPs use a multiplexed address and data bus to save on the number of package pins. A common way to interface these 8-bit µPs to 12-bit DACs is the double-buffer method, which transfers the low-order 8 bits first and then transfers the high-order bits. This method requires an external latch for the 8-bit data bus.

The circuit in **Fig 1** can transfer the same 12-bit word, but doesn't require an external data latch. The circuit uses the address latch, IC_1, and a short software routine **(Listing 1)** to transfer the four high-order bits of a 12-bit word to the address latch first, and to transfer the low-order 8 bits using one instruction. **EDN BBS /DI_SIG #1239**

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Listing 1—8-bit µP to 12-bit DAC transfer routine

```
mov  a,high_byte        ; assume xxxxDDDD DDDDDDDD as 12-bit
                        ; word    |-high-| |-low -|
mov  dpl,a              ; high order 4 bits to low data pointer
mov  dph,#7fh           ; set a15=0
mov  a,low_byte         ; low order 8-bit to accumulator
movx @dptr,a            ; output 12-bit word to 12-bit DAC
                        ; in one instruction
```

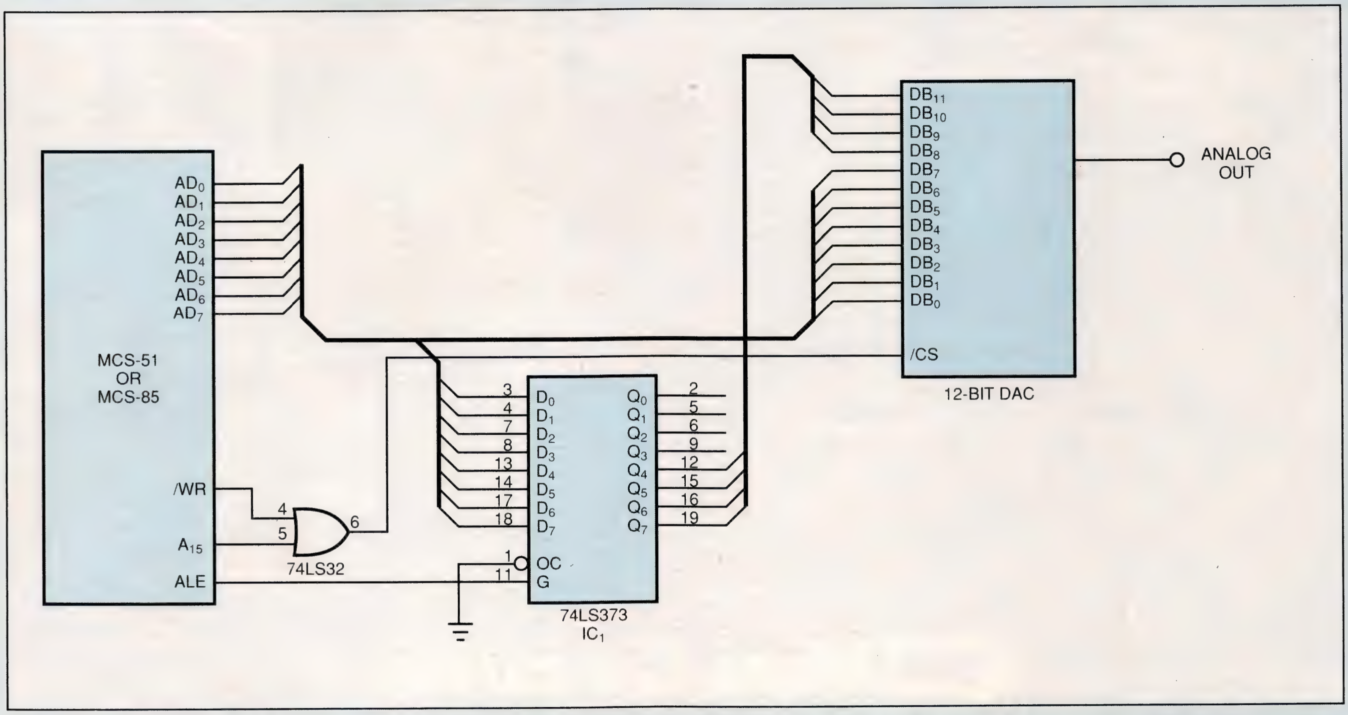

Fig 1—This circuit and a short software routine save an external data latch and use the address latch to transfer 12 bits of data from an 8-bit µP to a 12-bit DAC.

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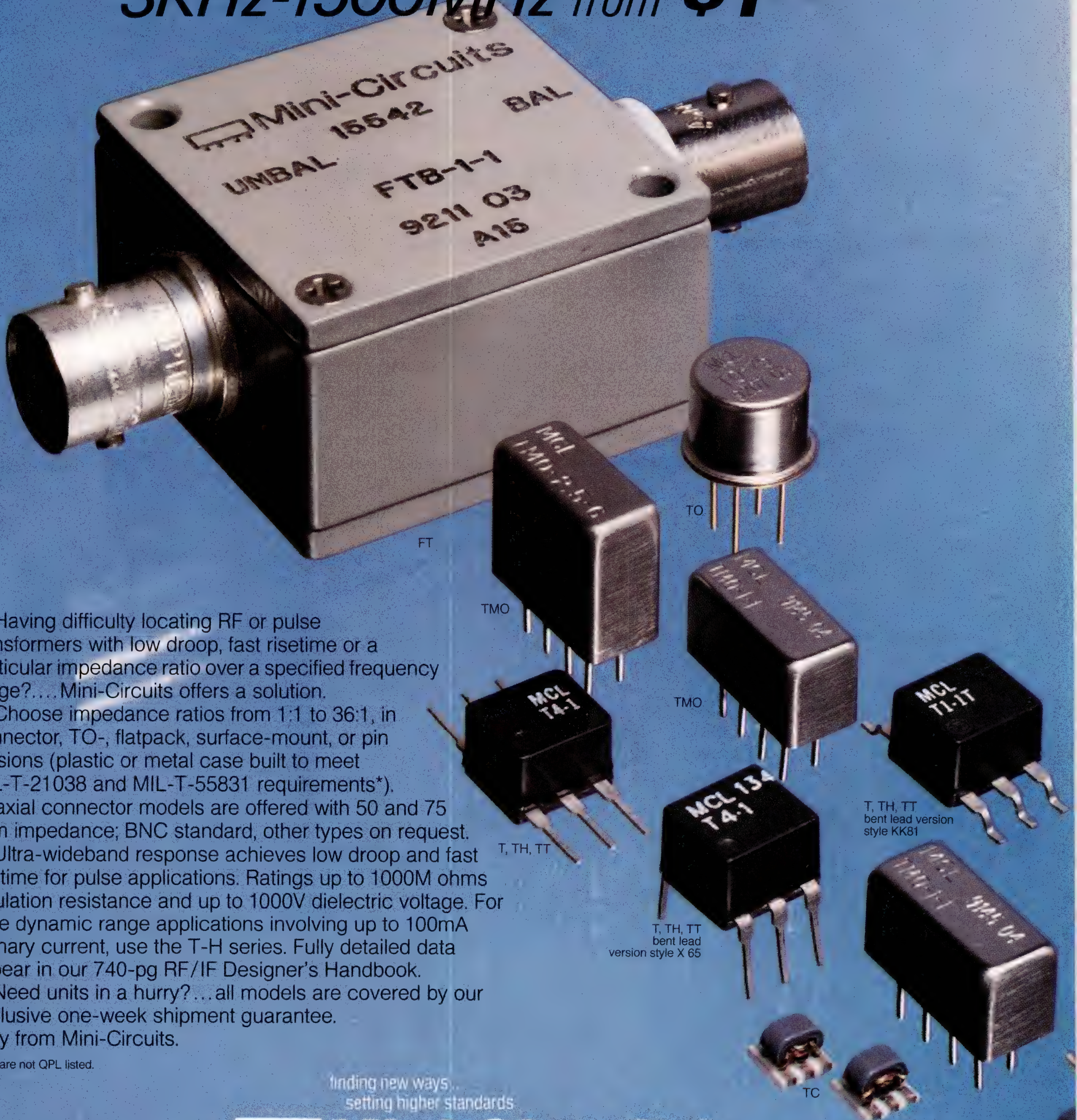

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CIRCLE NO. 73

F 71 REV. D

significant distortion occurs during the flat portions between peaks. The compensated waveform (trace D) recovers the low-frequency information and the peak current level.

Any spreadsheet can also implement the compensator. You need to import the ac current probe's waveform values from the scope, and you must know the sampling interval or time between points. The only trick is to implement the integration function (**Table 1**). If you put the waveform value, x(t), in column A, then you should create a second column, B, that represents the integral of x(t). Force the first cell to be 0, then each successive value is simply the previous value plus the present x(t) value times the sampling interval. Finally, create a third column, C, which sums the first column and ω times the second column. For **Table 1**, the sampling interval was 25 μsec and ω = 450.

Table 1—Spreadsheet for ac-current-probe compensation

	A	B	C
1	x(1)	0	= A1 + 450*B1
2	x(2)	= B1 + A2*25E − 6	= A2 + 450*B2
3	x(3)	= B2 + A3*25E − 6	= A3 + 450*B3
4	x(4)	= B3 + A4*25E − 6	= A4 + 450*B4
5	etc	etc	etc

Although the integration function is the key to this technique, it is also its greatest limitation. If your scope has a dc offset error, then the integrator will cause the compensated waveform to ramp up or down depending on the sign of the offset. You can correct for this by subtracting the offset from each x(t) value before computing the result. Experiment with the correction value until the ramp disappears. This technique works because you're constraining the constant of integration to 0 by measuring only start-up conditions and by correcting for dc offsets in the instrumentation.

When using this technique, use your probe within its operating limits. The magnetic properties of many ac current probes limit the amount of dc and pulsed currents that you can apply. This technique only compensates for the probe's low-frequency roll off. Correcting for magnetic saturation effects is a much more complicated problem. **EDN BBS /DI_SIG #1236**

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To Vote For This Design, Circle No. 392

Solid-state fuse resets itself

Isaac Eng, ESTCO Battery, Ottawa, Canada

The solid-state fuse in **Fig 1** automatically resets once current has returned to normal after an overcurrent condition. The circuit draws less than 350 μA with the fuse blown (Q_1 off) or not blown (Q_1 on). The circuit allows load currents up to 1A to flow, but drops into strobe mode with load currents that exceed 1A.

The LM10 op amp buffers the voltage of the current-sense resistor (R_1) to charge C_1 through a forward-biased D_1. Pin 8 of the LM10 compares C_1's voltage to the LM10's internal 0.2V reference. When C_1's voltage is less than 0.2V, the comparator output (pin 1) is high and keeps Q_1 turned on and conducting load current. When the load current exceeds 1A, the voltage across C_1 exceeds 0.2V. The comparator output goes low, Q_1 turns off, and load current is cut off. C_1 then discharges through the 3.3-MΩ resistor. When the voltage decreases below 0.2V, Q_1 turns on again

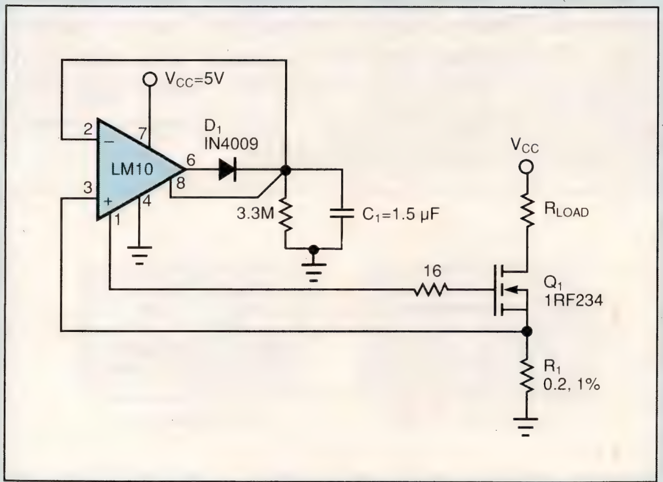

Fig 1—Based on the charge on C_1, the LM10's internal comparator determines the state of pin 1, which shuts off Q_1 if load current exceeds 1A.

EDITED BY CHARLES H SMALL & ANNE WATSON SWAGER

Software extends ac current probe's range

Stan Sasaki, Tektronix, Beaverton, OR

AC current probes based on current transformers don't pass dc information. This limitation typically forces you to use more expensive dc current probes to analyze asymmetrical start-up waveforms such as turn-on or in rush currents. However, you can use ac current probes by taking advantage of the zero initial value of start-up events to recover low-frequency information. The required processing software is available in some digital oscilloscopes and all PC spreadsheets.

An ac current probe has a conversion factor of kV/A (**Fig 1**). The probe's frequency response rolls off at its low-frequency pole, ω, set by the probe's transformer L/R time-constant or droop factor. An ideal compensator has a transfer function with a zero at ω and a pole at dc. You can implement this compensator using the following equation:

$$y(t) = x(t) + \omega \cdot \int x(t) \qquad \textbf{(1)}$$

Thus, if the ac current probe's waveform is x(t), then compute the compensated output by adding x(t) to ω times the integral of x(t). The only parameter you need is ω. Some ac current probes specify the roll-off frequency in Hz ($\omega = 2\pi f$), but it's best to measure the value. Simply apply a dc current step and measure the decay time, τ, or the time it takes for the probe's output to fall to 37% of its peak value. Then, $\omega = 1/\tau$.

Some digital scopes have a built-in integration function that let you define a new waveform that directly implements the compensator. **Fig 2** shows voltage and current waveforms (traces A and B, respectively) on a disk drive's 5V supply. A dc current probe is the reference. Trace C is the output from an ac current probe. The probe's roll-off frequency was measured as just above 70 Hz, so $\omega = 450$. The scope calculated trace D using **Eq 1**. Notice how the compensator recovers the low-frequency information.

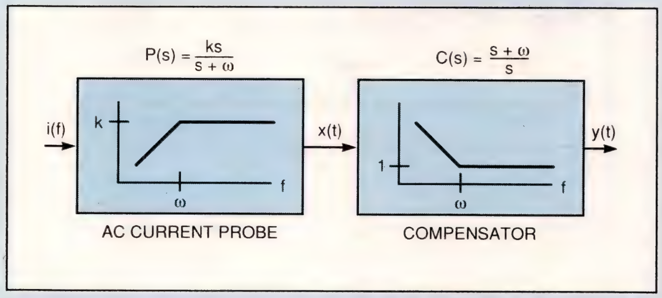

Fig 1—An ac current probe's response falls off at low frequencies, but a compensator with a pole at dc and zero at the probe's low-frequency cut off can theoretically extend the response to dc.

Fig 3 shows the start-up waveforms of a switching power supply. The dc current probe shows a peak current of −10A (trace B). The uncompensated ac current probe's reading (trace C) is low due to droop, and

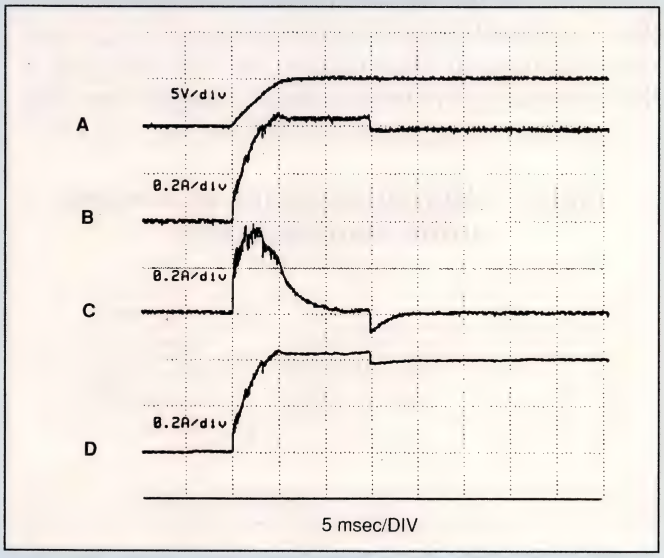

Fig 2—A dc-probe's measurements of a disk-drive's 5V start-up voltage and current (traces A and B, respectively) don't match the measurements of an ac current probe (trace C) until the compensation is included (trace D).

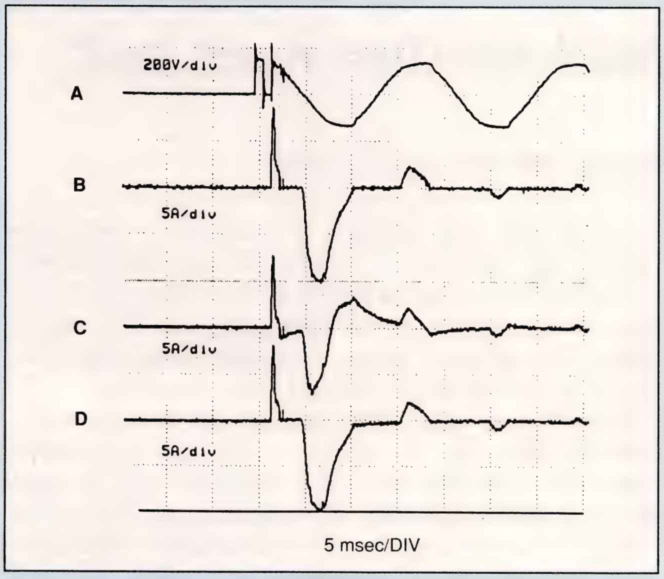

Fig 3—The compensated ac-current-probe measurement of a switching power supply's power-line voltage and current (trace D) improves upon the uncompensated ac measurement (trace C) by showing the true negative peak current level and removing the distortion. Traces A and B are the dc-probe measurements of voltage and current, respectively.

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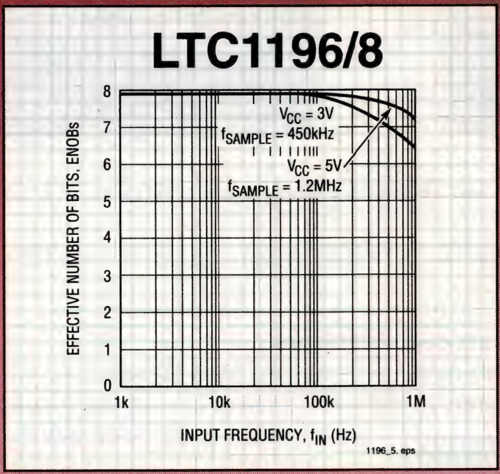

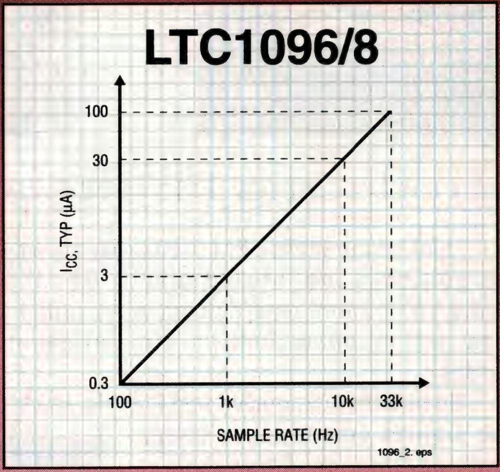

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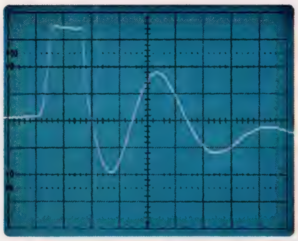
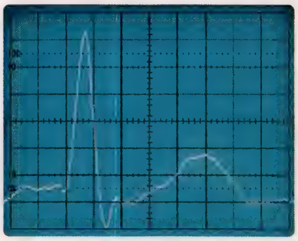
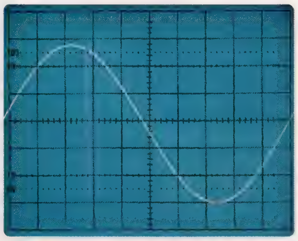

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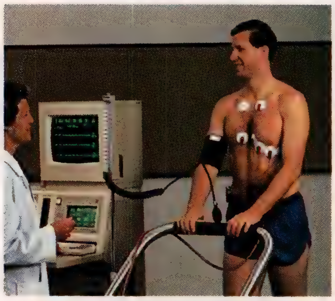


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oped DSP-based waveform synthesizer to incorporate the DNG algorithm. Thus, we had a composite real-time signal consisting of MF tones plus Gaussian noise to use as a source. We used an already existing user interface to vary the levels of the tones and noise.

Table 1 shows the results of the MF decoder performance for the DNG versus the GenRad 1390B, which is a commercially available random noise generator. In all cases, we used nominal MF frequencies, and the level of each tone was set to -22 dBm at 600Ω. The MF tone-switching rate was 70-msec ON and 70-msec OFF.

Both noise sources performed equally well for a noise level of -30 dBm, which actually exceeds the LSSGR requirements. We then raised the noise level to cause the MF decoder to fail (ie, miss digits). The two noise sources differ by 8.5% for the noise level required to produce the same MF decoder-error rate. After accounting for variations in the hardware test configurations, approximately a 5% difference remains between the DNG and 1390B noise levels. The internal structural differences of the noise sources themselves appear to be the cause of this difference. For this test case, the MF decoder appears to tolerate a slightly higher level of Gaussian noise from the DNG than the 1390B, for a given detection error rate.

The 16-bit, fixed-point DNG real-time performance compared favorably to that of a commercially available noise generator for moderate DSP sample rates. The fixed-point DNG performance is probably adequate for those applications where the accuracy of the random distribution is not of paramount importance. The DNG algorithms can offer a flexible and cost-effective solution for random noise generation, especially in those applications where you are already using DSP techniques.

You could increase the DNG's noise bandwidth if you increased the sample rate. However, this increase impacts hardware cost, especially for the DAC and the output lowpass filter needed. The commercial unit used for comparison here can generate noise up to 5 MHz in bandwidth.

A major deficiency of the fixed-point DNG is the relatively small word length. **Ref 1**, for example, recommends that the word length be at least 30 bits. Another deficiency has to do with the dynamic range (overflow and scaling considerations). You could address both of these deficiencies by using a 32-bit, floating-point DSP chip. However, floating-point DSP devices are typically slower and more expensive than their fixed-point counterparts.

Increasing the batch size would improve the distribution of the Gaussian sequence at the expense of increased computational load. The tradeoff is between the accuracy of the output distribution and the DSP chip's speed. This tradeoff ultimately limits the bandwidth of the resultant noise signal. EDN

Table 1—DNG output sequence values

	Uniform x(n)		Gaussian g(n)	
Iteration, n	Hex Value	Decimal Value	Hex Value	Decimal Value
1	66B7	26295	347F	13439
2	1588	5512	340F	13327
3	1D75	7541	379F	14239
4	2C8E	11406	372F	14127
5	5EA3	24227	4ABF	19135

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Acknowledgment

The author would like to express appreciation to Dr Ken Boudwin of Exxon Research and Engineering, Florham Park, NJ, for his help in understanding the statistical tests for randomness, and to Sherrie Gumienny, English Department Head for Life Center Academy, Burlington, NJ, for her review and helpful comments of the article.

Author's biography

Bill Salibrici is a Principal Member of the Technical Staff of TeleSciences Co Systems, Moorestown, NJ, a supplier of operation-support systems for telephone companies worldwide. For the past five years, he has been responsible for development of DSP software for real-time, voice-band applications. Bill has a BSEE from Pennsylvania State University, University Park, PA, and has taken graduate studies from the University of Pennsylvania, Philadelphia, PA.

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However, the MSB cycles with a full period. Therefore, the sequence **Eq 3** generates has a full period of length m (ie, the sequence repeats after m values).

Fig 2 shows the algorithm used to implement **Eq 3** for uniformly distributed pseudo random numbers. Notice that **Eq 3** is partitioned so that $[a \times x(n)] \bmod m$ is calculated first, and then the modulo m addition to c is done. **Fig 3** shows the algorithm used to implement **Eq 2** for Gaussian-distributed pseudorandom numbers. The batch size for Gaussian noise was 16, and the uniformly distributed random numbers come from **Eq 3**. Notice here that each element of the summation is divided by the batch size before adding it to the running sum. You do this to prevent overflow errors. You can easily apply these algorithms to other single-chip DSP devices with perhaps minor changes due to architectural differences.

Listing 1 shows the source code used to implement the Uniform algorithm on the 77P25. **Listing 2** shows the source code used to implement the Gaussian algorithm. The **Listing Table** shows the first five numbers, in integer format, of the Uniform and Gaussian output sequences. (Both **Listings** and the **Listing Table** are located on the EDN BBS.)

Evaluating the results of several simulation programs addressed the question of how random the DNG is. These simulations showed that the raw DNG noise distributions have the expected shape. The results of two statistical tests for proper fit indicate that the hypothesis of normality for the Gaussian case is accurate. The autocorrelation function of the DNG compared to the drand48 function (a function Sun Microsystems Inc's C Library provides) are slightly different, but not radically so.

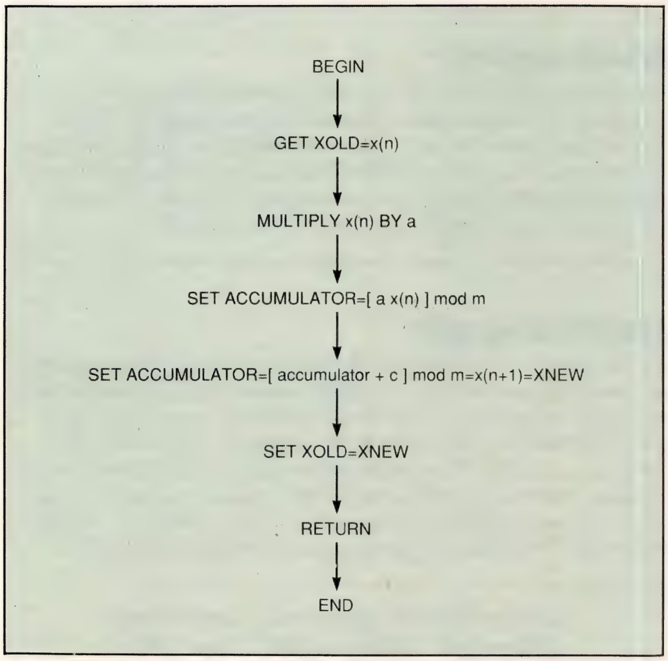

Fig 2—You can generate uniformly distributed, pseudorandom numbers with the program illustrated here.

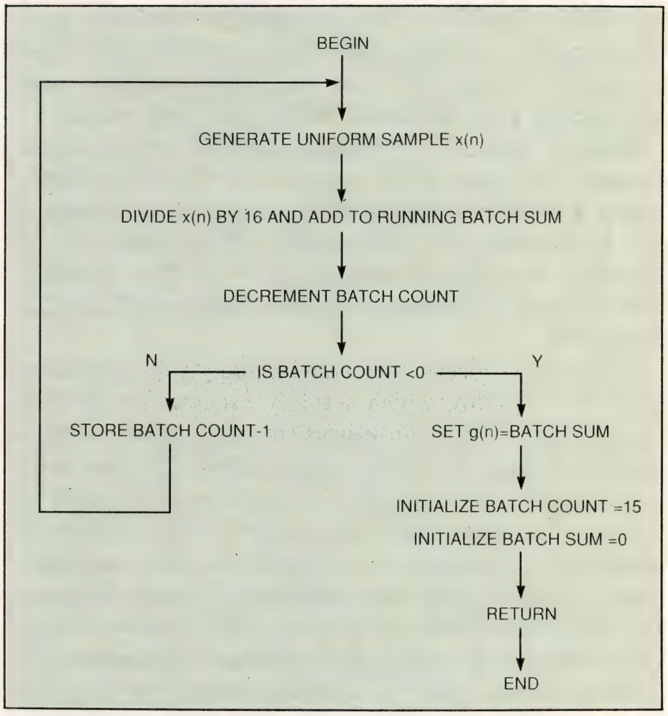

Fig 3—You can generate Gaussian-distributed, pseudorandom numbers by taking the output of the uniform algorithm described in Fig 2 and following this flowchart.

We performed further tests using the hardware design shown in **Fig 1**. We scaled the internal DNG random numbers for a zero mean by subtracting ½ and expanded them to full scale by multiplying by 2 so that the DSP chip's output range was between -1 and $+1$. In order to use the codec DAC, we performed a linear-to-μlaw software conversion before outputting the noise sample. A lowpass filter inside the codec band limits the analog noise output signal to approximately 3 kHz. The codec output has a full-scale excursion of ± 3V, which introduces a voltage gain factor of 3 between the DSP chip's output and the final analog output.

These lab tests showed that the measured values for the mean and variance are close to theoretical values. Also, the Gaussian frequency spectrum of the DNG compares well to that of a commercially available noise generator for the 3-kHz band-limited case.

We needed the Gaussian noise source in order to test the detection of multifrequency (MF) tones in the presence of Gaussian noise. The Bell Communication Research LSSGR (**Ref 6**) defines the required MF decoder performance. We modified our internally devel-

(least significant bits) of X. For example, $(a \times X) \bmod m$ is simply the product $(a \times X)$ truncated to m LSBs.

One method to generate a Gaussian (or normal) distributed random-number sequence is to apply the Central Limit Theorem to batches of uniformly distributed random-numbers (**Refs** 3 and 4). You can mathematically express this idea as follows:

$$g(n) = \frac{1}{B}\sum_{i=0}^{B-1} x(i), \qquad (2)$$

where the x(i) are uniformly distributed, independent random numbers; B is the batch size; and g(n) is a member of a set of random numbers approximately Gaussian distributed.

This algorithm produces a pseudorandom sequence whose distribution is close to Gaussian, provided that the batch size B is greater than 10. If you choose a power of 2 as your batch size, then you can use a shift-right operation to simplify the required division within the DSP chip.

The data representation internal to the 77P25 is the 16 bit, two's-complement, fractional format. This means that the most significant bit (MSB) is the sign bit followed by an implied binary point. The remaining 15 bits contain the fraction magnitude. You can represent the range of numbers -1.0 to $(1-2^{-15})$ in this format, or you can express them with hexadecimal numbers as 8000H to 7FFFH.

To apply the linear congruential generator in this case, we used $m = 2^{15}$, which is the size of the fraction magnitude. Then **Eq 1** will generate positive integers between 0 and 32768.

However, the interpretation of these integers is x(n)/m, so that the end result will be a sequence of numbers that lie between 0 and 1. **Refs 1**, **2**, and **5** discuss some criteria for choosing the four constants of **Eq 1**. The modulus m should be as large as possible so that the sequence it generates has a long period. The multiplier a should lie between 0.01 and 0.99 m, such that a mod 8=5. For example, a value of a=9821 satisfies this criteria. The increment c is immaterial when a is a good multiplier, except that it must have no factor in common with m. For example, a value of c=6925 satisfies this criteria.

You may arbitrarily choose the seed value x(0). Notice that a given seed value will exactly reproduce the same stream of random numbers. This feature may be useful in those applications where identical random numbers would yield a more precise comparison of the performance of different systems. For most of this article's data, 11186 is the seed value, although several other values were also tested. The linear congruential generator now becomes:

$$x(n+1) = [9821 \times x(n) + 6925] \bmod 2^{15}. \qquad (3)$$

The LSBs of the numbers **Eq 3** generates are not very random, but cycle with regular patterns. This nonrandom behavior is characteristic of all generators of **Eq 1**'s form, where m is some integer power of 2.

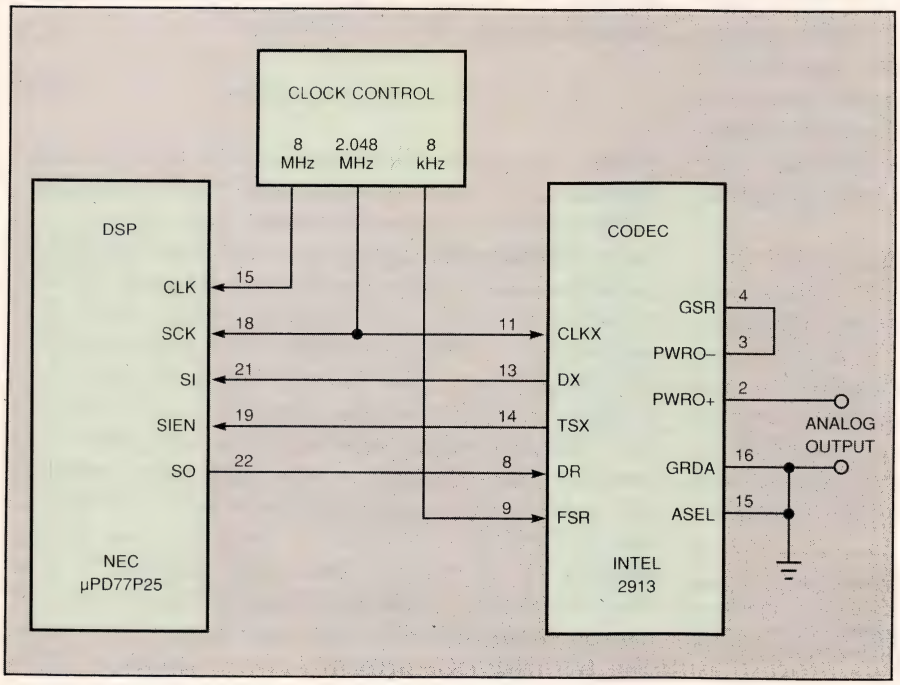

Fig 1—To test the noise produced by the DNG algorithm, we used an existing platform that included the DSP and codec.

Fixed-point DSP chip can generate real-time random noise

Bill Salibrici, TeleSciences Co Systems

An inexpensive, 16-bit, fixed-point DSP chip can generate real-time pseudorandom noise signals for testing the performance of telephony systems in the presence of noise.

As device costs drop and development support grows, DSP chips are finding use in diverse applications, such as in real-time digital waveform synthesis. Increased DSP use raises two questions: Can you exploit the fast multiply-accumulate capability of single-chip DSP devices to generate real-time random noise samples, and, if so, how would the performance compare to a commercially available noise generator? To answer those questions, we wrote and tested a DSP application. This application required a signal plus random noise, as is often needed in testing digital filters used to implement tone detection. We developed the digital noise generator (DNG) algorithm to generate real-time, pseudorandom, uniformally or Gaussian-distributed signals.

We used the µPD77P25, a 16-bit fixed-point DSP chip from NEC Electronics, to test the DNG algorithm. The chip is a second-generation, medium-speed, single-chip device. We chose the chip out of convenience; the hardware platform from an existing application was already available. However, the concepts presented in this article are applicable to other fixed-point, as well as floating-point, DSP chips. **Fig 1** shows a block diagram of the hardware used to test the algorithm.

Software listings for this article are available on EDN's computer bulletin-board system (BBS). Phone (617) 558-4241 with modem setting 300/1200/2400 8,N,1. Access */freeware* SIG and specify *(r)ead* option followed by *(k)eyword* search for "MS #530".

The µPD77P25 has a serial output port that can interface to a simple, low-cost codec, which we used as a DAC.

The codec also contains internal antialiasing filters, which further simplifies the hardware. Other fixed-point DSP chips that include a serial output port are the Analog Devices ADSP-2101, AT&T DSP16, Motorola DSP56000, and Texas Instruments TMS320C25. The sample rate used here is 8 kHz, which means that the highest frequency component contained in any synthesized output waveform must be band limited to 4 kHz or less to prevent aliasing errors.

The linear congruential generator (**Refs 1** and **2**) was used to generate a uniformly distributed random-number sequence given as follows:

$$x(n+1) = [a \times x(n) + c] \bmod m, \qquad (1)$$

where a, c, and m are constants; mod is the modulus operator; $n \geq 0$; and x(0) is the seed or starting value.

For properly chosen constants and a given seed value, this algorithm produces a uniformly distributed, pseudorandom sequence of positive integers between 0 and m. The term pseudorandom simply means that you use a deterministic method to generate a sequence of numbers that appear to be independent draws from a uniform distribution. **Eq 1** basically states that you can obtain the next value in the sequence from the previous value through several operations, including the multiply-add combination for which DSP devices are well suited. The modulus operator gives the remainder of one number divided by another. If m is chosen to be the word size of the DSP chip, then the modulo m operation becomes quite simple. The operation (X) mod m is accomplished by taking m LSBs

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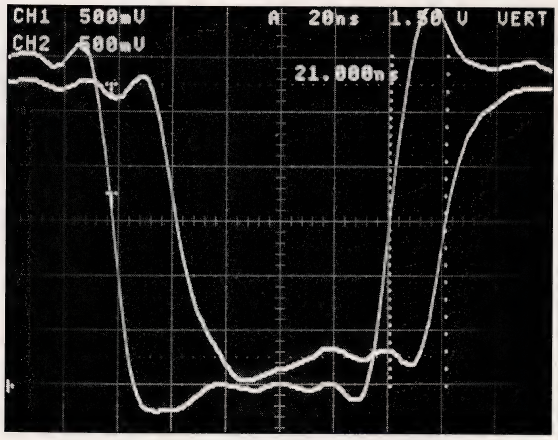

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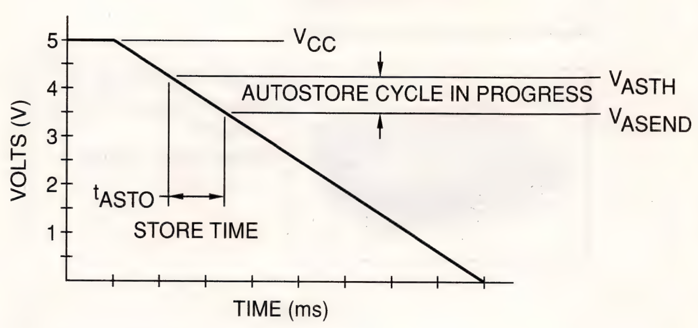

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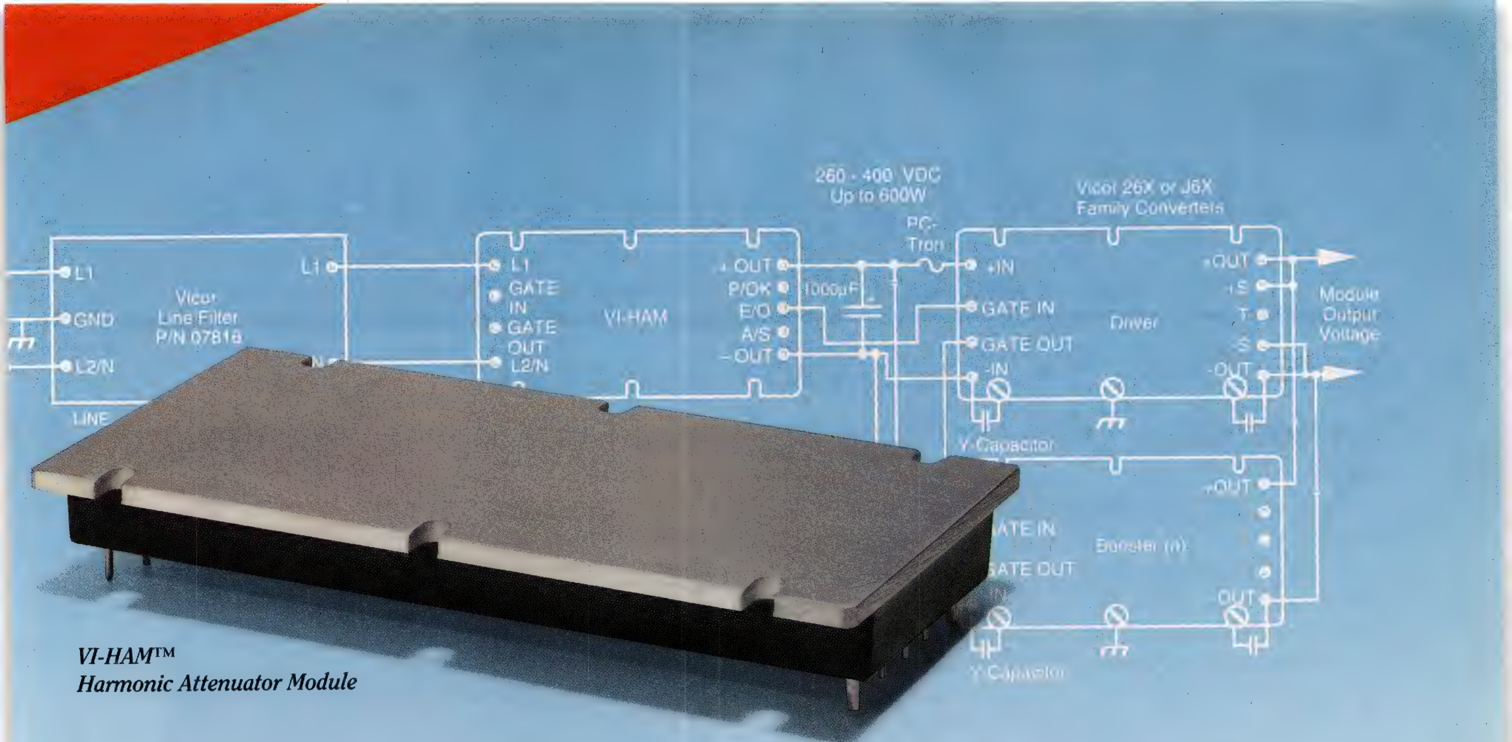

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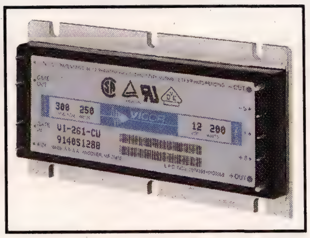

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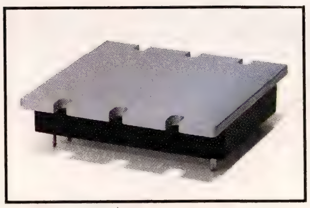

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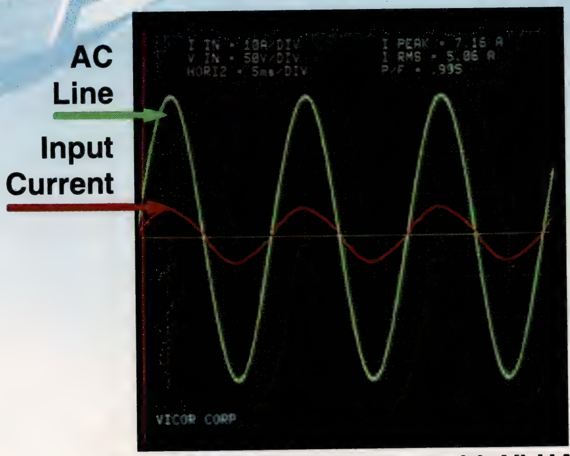

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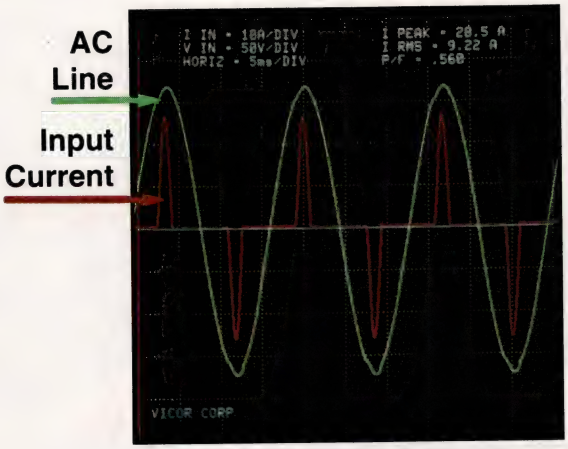

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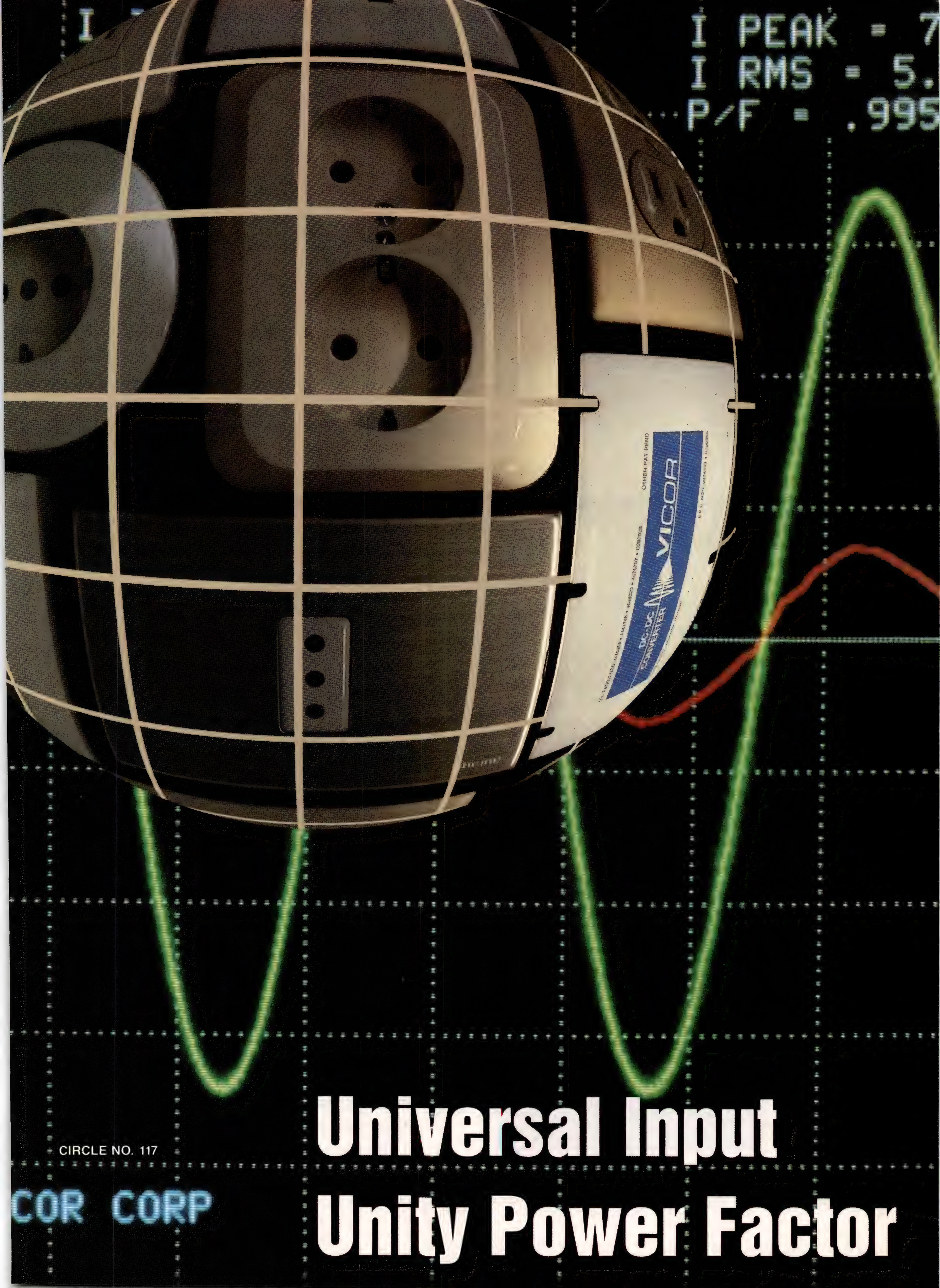
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shows an 8-pole, lowpass Butterworth filter constructed with four Sallen and Key (**Refs** 4 and 5) lowpass filters. A common perception is that multiple-pole filters produced in volume will not perform reliably because of component variation. The concern is that component variation will distort a filter's performance; poles will shift so much that the filter will no longer be a true Butterworth filter. Monte Carlo analysis can investigate this concern.

Listing 2 models **Fig 4**'s filter circuit using 10% capacitors and 1% resistors, both with uniform distributions. Again, high-gain voltage-controlled voltage sources replace op amps to simplify the PSpice model. The .AC directive specifies the frequency domain, which is well suited for analyzing filters. The .PROBE directive specifies PSpice's graphical output.

The filter's simulated gain appears in **Fig 5**. The curves are from three of 25 simulation runs: the run with nominal component values, the run with the lowest gain, and the run with the highest gain. Although the cut-off frequency varies, the filter appears to behave like a Butterworth filter.

Monte Carlo analysis helps you understand the effects of component tolerances on circuits without having to rely on rules of thumb or guesses. Because you'll understand these effects before a circuit goes into production, you can correct many problems in the design phase. And depending on the version of Spice you use, your current circuit models should require only a few changes to let you analyze performance using Monte Carlo techniques. EDN

Listing 2—Simulation model for an 8-pole Butterworth filter

```
V1 1 0 AC 1.0V                 ;Input signal is 1 volt

R1 1 2 ONE_PERCENT_R  31.6K    ;Sallen and Key Filter #1
R2 2 3 ONE_PERCENT_R  14.3K
C1 2 4 TEN_PERCENT_C 0.082UF
C2 3 0 TEN_PERCENT_C 0.068UF
E1 4 0 (3, 4) 1000K

R3 4 5 ONE_PERCENT_R  22.1K    ;Sallen and Key Filter #2
R4 5 6 ONE_PERCENT_R  16.9K
C3 5 7 TEN_PERCENT_C 0.1UF
C4 6 0 TEN_PERCENT_C 0.068UF
E2 7 0 (6, 7) 1000K

R5 7 8 ONE_PERCENT_R  31.6K    ;Sallen and Key Filter #3
R6 8 9 ONE_PERCENT_R  13.7K
C5 8 10 TEN_PERCENT_C 0.15UF
C6 9 0 TEN_PERCENT_C 0.039UF
E3 10 0 (9, 10) 1000K

R7 10 11 ONE_PERCENT_R  37.4K  ;Sallen and Key Filter #4
R8 11 12 ONE_PERCENT_R  14.7K
C7 11 13 TEN_PERCENT_C 0.39UF
C8 12 0 TEN_PERCENT_C 0.012UF
E4 13 0 (12, 13) 1000K

.MODEL    ONE_PERCENT_R  RES(R=1 DEV=1%)    ;1%  uniform distribution
.MODEL    TEN_PERCENT_C CAP(C=1 DEV=10%)    ;10% uniform distribution

.AC DEC 50 30 300                           ;50 points/decade, 30 to 300 Hz
.MC 50 AC V(13) YMAX LIST OUTPUT ALL        ;50 runs. Monitor V(13) using
                                            ; YMAX collating function

.PROBE V(13)                                ;Specify PSpice "oscilloscope"

.END
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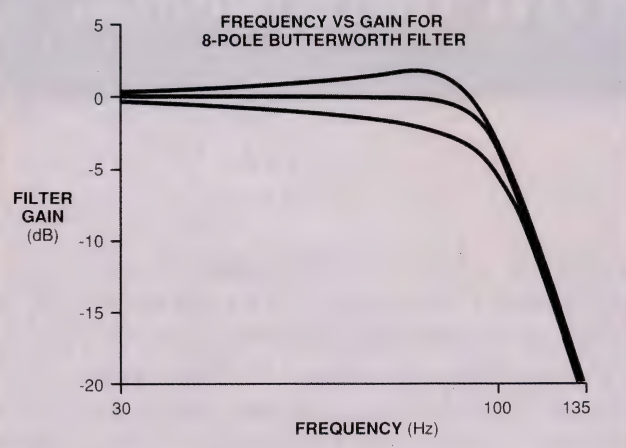

Fig 5—The simulated gain for Fig 4's circuit shows that the circuit does, as intended, behave like a Butterworth filter. The plot shows the results from three of the 25 simulation runs: the run with nominal component values, the run with the lowest gain, and the run with the highest gain.

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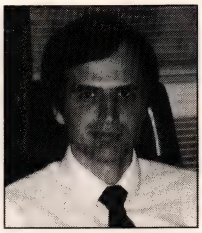
Author's biography



George Ellis is manager of new product engineering at Kaydon Corp in Blacksburg, VA, where he concentrates on developing data-acquisition systems. George is the author of Control System Design Guide *(Academic Press Inc, Orlando, FL, 1991). He has BSEE and MSEE degrees from Virginia Polytechnic Institute and State University (Blacksburg, VA).*

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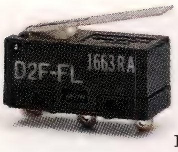

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CIRCLE NO. 92

SIMULATING COMPONENT VARIATIONS WITH SPICE

To compare the many simulations mathematically, Monte Carlo methods use collating functions. Spice programs let you choose a collating function according to the measure of performance you consider most important. For example, if you're simulating a switching circuit, you might want to know when a rising edge occurs. In this case, you can specify that the time of the edge be recorded for each simulation. Different versions of Spice offer different collating functions; for example, PSpice has five to choose from. However, you can choose only one function for per Monte Carlo analysis.

The following examples use an intuitive collating function, called YMAX, which compares simulations. The first simulation run uses nominal values for each component; subsequent runs use random numbers to generate values for all components and their tolerances. The value of YMAX results from comparing the output waveform of each run to that of the first, or nominal, run. The YMAX value is the point of greatest difference between the two waveforms.

Listing 1—Simulation model for cascaded op amps

```
V1 1 0 1.00                            ;Input signal is 1 volt D.C.

R1 1 2 ONE_PERCENT_R  1K               ;Gain stage #1
R2 2 3 ONE_PERCENT_R  1K
E1 3 0 (0, 2) 1000K

R3 3 4 ONE_PERCENT_R  1K               ;Gain stage #2
R4 4 5 ONE_PERCENT_R  1K
E2 5 0 (0, 4) 1000K

R5 5 6 ONE_PERCENT_R  1K               ;Gain stage #3
R6 6 7 ONE_PERCENT_R  1K
E3 7 0 (0, 6) 1000K

.MODEL    ONE_PERCENT_R  RES(R=1 DEV=1%)  ;1% uniform distribution

.DC V1  0.0 1.0 1.0                        ;D.C. analysis at 0 and 1 volt
.MC 250 DC V(7) YMAX LIST OUTPUT ALL       ;250 runs.  Monitor V(7) using
                                           ;YMAX collating function

.END
```

Analyzing circuits

Two examples illustrate Monte Carlo analysis. The first considers the effects of cascaded gain stages; the second examines the effects of component variation in a high-pole-count analog lowpass filter.

A common question among engineers concerns a cascaded op-amp circuit such as the one in **Fig 3**: If each of the six resistors has 1% tolerance, how much should you expect the overall gain to vary? The easy answer is to assume the worst case: ±6%. This would occur if R1, R3, and R5 were 1% low, and R2, R4, and R6 were 1% high. It is unlikely that this combination would ever occur, but how much variation would be likely to occur? Monte Carlo analysis answers just such questions.

Listing 1 contains a model for the Monte Carlo analysis of the circuit in **Fig 3**. Note that high-gain voltage-controlled voltage sources replace the op amps in order to simplify the PSpice model. Note also that only a few lines make up the Monte Carlo model: an .MC line specifying 250 simulations and the YMAX collating function, and a .MODEL line specifying uniformly distributed ±1% resistors.

Simulations using this model show that circuit gain varies much more than ±1%. The greatest variation over 250 simulations is +3.9%, and the gain from seven simulations (of 250) varied more than ±3%.

The results are very different, however, when the circuit's resistors have a normal, rather than uniform, distribution. To change the distribution, you need only modify the .MODEL line to

.MODEL ONE_PERCENT_R RES(R=1
DEV/GAUSS=0.25%)

With this change, the greatest variation in circuit gain over 250 simulation runs is +1.8%, and only 21 runs show gains that vary more than ±1%.

Simulating the effects of component variation in a filter is another use for Monte Carlo analysis. **Fig 4**

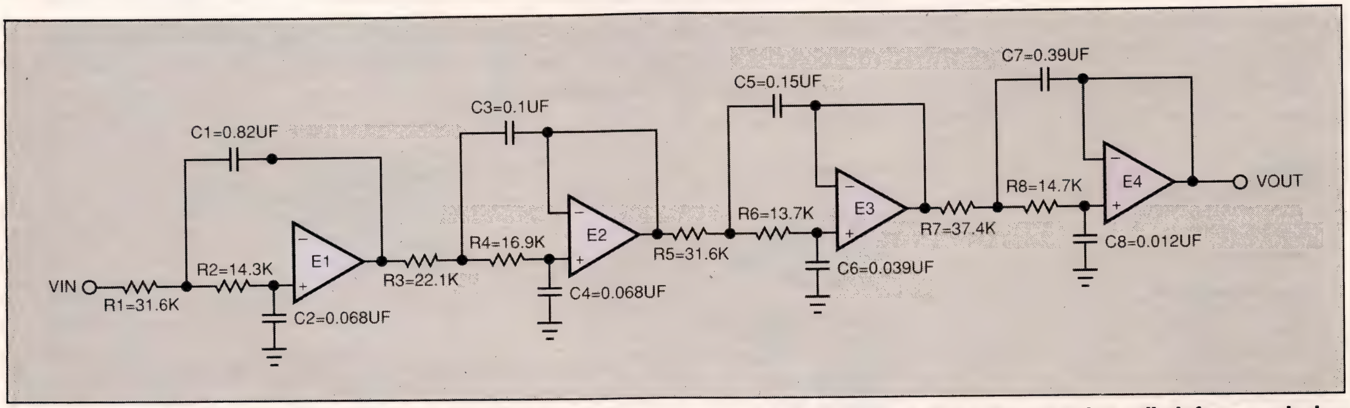

Fig 4—For this 8-pole, lowpass Butterworth filter, Monte Carlo analysis can help determine if the filter's poles will shift so much that the circuit will no longer be a true Butterworth filter.

large volume, you would probably specify a normal distribution. However, if you're using components that have been discriminately selected from a low-yield batch, the distribution will be closer to uniform.

For example, manufacturers may select capacitors with ±20%, ±10%, and ±5% tolerances from one manufacturing batch. The selected capacitors have a somewhat uniform distribution (**Fig 2a**); however, the remaining capacitors have a distribution with a "notch" (**Fig 2b**). To account for a distribution such as this, you have to specify the distribution yourself.

In PSpice, you can divide custom distributions into as many as 100 parts, each part being a section of the distribution curve. You specify the distribution with two *x,y* pairs for each part. For example, you can specify a 5-part distribution for ±20% capacitors (**Fig 2c**) by using the following statements:

```
.MODEL TWENTY_PERCENT_C CAP(C=1
  DEV/BI_MODAL 20%)
.OPTIONS DISTRIBUTION=BI_MODAL
.DISTRIBUTION BI_MODAL (-1, 0) (-0.5, 1) (-0.5, 0)
  (0.5, 0) (0.5, 1) (1, 0)
```

One problem with statistical analysis is that component manufacturers usually don't provide distributions. One lot of 20% capacitors may contain a substantial number of 10% capacitors because the manufacturer produced more than enough 10% capacitors to fill orders; the next lot may not have any 10% capacitors.

If you don't know the distribution, you can take a guess; uniform distribution will usually provide reasonable results. If you're especially concerned about a component, you can contact the manufacturer, but don't expect much help. The manufacturer may provide guidance but probably won't make any commitments.

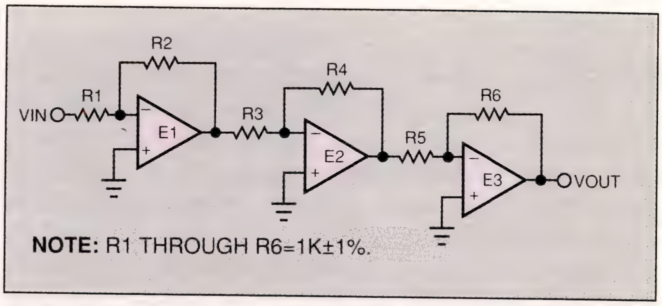

Fig 3—In a cascaded op-amp circuit, the tolerances of the resistors combine to affect the circuit's gain. In the worst case, the gain varies by ±6%; however, it's likely that the actual variation will be less.

Spice programs such as PSpice use Monte Carlo analysis to investigate component variations. Monte Carlo analysis, as its name implies, is based on chance. It involves using random numbers in a calculation that has the structure of a statistical, not deterministic, process (**Ref 3**).

Monte Carlo methods often fall into two categories: solution and simulation. Solutions directly solve a problem, such as determining the numerical value of π. Monte Carlo methods for circuit analysis are in the second category—simulations.

The effects of component tolerances on circuit performance are statistical, and those effects can be characterized by simulating a circuit multiple times. Each time, the simulation generates random numbers to create new values for components with tolerances. The combination of many simulations predicts the range of performance you can expect from the circuit.

Spice programs with Monte Carlo analysis

Spice programs that include Monte Carlo analysis are available from several vendors, and some programs are available in modestly priced evaluation versions. Evaluation versions let you experiment before buying a complete package. They usually do everything, or almost everything, that production versions do, but they limit the size and complexity of circuits you can simulate.

For information about Spice programs that feature Monte Carlo analysis, contact the following companies:

Intusoft
2525 S Western Ave, Suite 203
San Pedro, CA 90732
(301) 833-0710
Circle No. 351

Meta-Software Inc
1300 White Oaks Rd
Campbell, CA 95008
(800) 346-5953
Fax (408) 371-5100
Circle No. 352

Microsim Corp
20 Fairbanks
Irvine, CA 92718
(800) 245-3022
Fax (714) 770-3022
Circle No. 353

Spectrum Software
1021 S Wolfe Rd
Sunnyvale, CA 94086
(408) 738-4387
Circle No. 354

Tatum Labs Inc
3917 Research Park Dr, Suite B-1
Ann Arbor, MI 48108
(313) 663-8810
Circle No. 355

any model by following the parameter with "DEV=nn%". For example, a transformer (K) can have a variable-effective air gap if you add the lines

```
K1 1 2 3 4 VARIABLE_AIR_GAP 100UH
.MODEL VARIABLE_AIR_GAP CORE
  (GAP=0.1 DEV=5%)
```

Here, the air gap is 0.1 cm ±5%.

Sometimes, parameters vary in groups. PSpice provides the LOT directive for these cases. For example, suppose you're using a resistor pack with eight resistors that you know have a tolerance of ±1% and are matched to be within 0.2% of each other. The resistor model would be

```
.MODEL ONE_PERCENT_RPAK RES(R=1
  DEV=.02%
  LOT=.08%)
```

With this model, you can specify eight resistors in your circuit. (Actually, this same statement can specify any number of resistors in a pack.) The values of the eight will vary ±1% from one run to the next, but on any given run, they will vary only ±0.2% from each other. If the circuit has more than one resistor pack, you need a .MODEL directive for each one. These directives let the resistances of one pack vary from the resistances of a second pack by the full ±1%.

A component's tolerance describes only the limits of variation. For a complete description, you must also know the statistical distribution—how likely a component is to take on a particular value. (Distribution is actually the integral of density. However, it is common to refer to a graph of statistical density as a "distribution," and the examples used here follow that conventional usage.)

The simplest distribution is uniform **(Fig 1a)**, in which components are equally likely to take on any value within the tolerance band. PSpice defaults to uniform distributions. PSpice also supports Gaussian, or normal, distributions **(Fig 1b)**, which are the most common distributions in manufacturing.

Gaussian distributions are described by two parameters: the mean, or average (usually represented by $\bar{x}$ or μ), and the standard deviation (σ). Components with normal distributions are much more likely to take on values in the center of the tolerance band rather than at the outside edges.

You can specify a normal distribution for ±1% resistors with the PSpice command

```
.MODEL ONE_PERCENT_GAUSS_R RES(R=1
  DEV/GAUSS=0.25%)
```

Here, the resistor values have a normal distribution and $\sigma=0.25\%$. PSpice limits values of normal distributions to $\pm 4\sigma$, so ONE_PERCENT_GAUSS_R can vary ±1%.

Manufacturing tolerances usually have normal distributions, so if you're using a component produced in

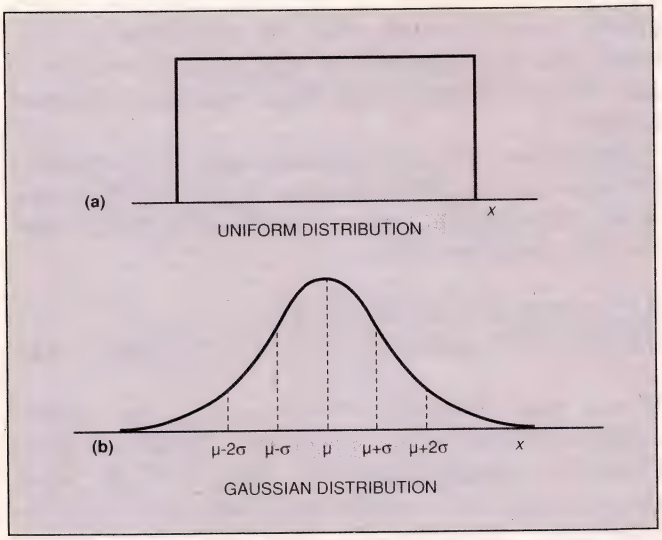

Fig 1—If the statistical distribution of components is uniform (a), then component values are equally likely to have any value within their tolerance band. The Gaussian, or normal, distribution (b) is the most common distribution in manufacturing, however.

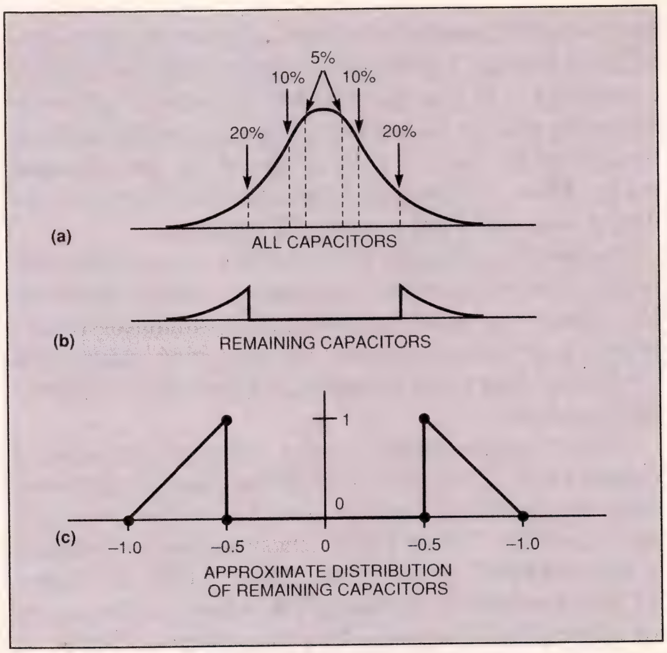

Fig 2—Capacitors with a specified tolerance may have a somewhat uniform distribution that doesn't include the Gaussian curve's "tails" (a). After those capacitors have been removed from a manufacturing batch, the remaining capacitors have a distribution with a "notch" in the middle (b). To account for distributions such as this one in Spice, you have to specify the distributions yourself (c).

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Numerical Computation

```
In[1]:=
3^70
Out[1]=
2503155504993241601315571986085849
In[2]:=
Hypergeometric2F1[7, 5, 4.1, 3-I]
Out[2]=
-0.00403761 - 0.00295663 I
```

Symbolic computation: Equation solving, symbolic integration, differentiation, power series, limits. Algebraic operations, polynomial expansion, factorization, simplification. Operations on matrices, tensors, lists, strings.

Symbolic Computation

```
In[1]:=
Integrate[x / (a + Exp[x]), x]
Out[1]=
```

$$\frac{x^2}{2\,a} - \frac{x\ \mathrm{Log}[1 + \frac{E^x}{a}]}{a} - \frac{\mathrm{PolyLog}[2, -(\frac{E^x}{a})]}{a}$$

Graphics and sound: 2D, 3D plots of functions, data, geometrical objects. Contour, density plots. 3D rendering with intersecting surfaces, lighting models, symbolic descriptions. Color PostScript output, combining and labeling, publication quality graphics, animation (most versions). Sound from waveforms and data (most versions).

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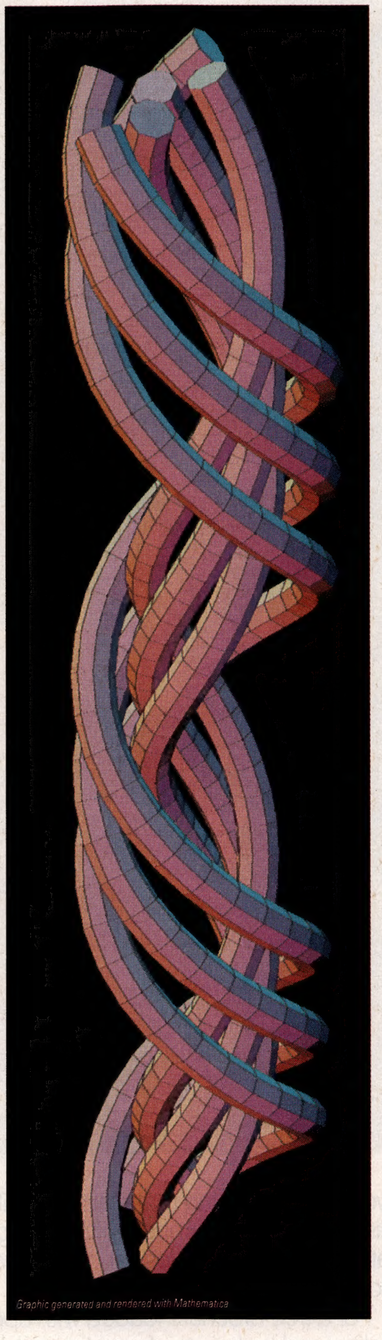

Graphic generated and rendered with Mathematica

Programming

```
log[1] = 0
log[E] = 1
log[x_ y_] := log[x] + log[y]
log[x_ ^n_] := n log[x]
log'[x_] = 1/x (* derivative *)
log/: InverseFunction[log] = exp
log/: Series[log[x_], {x_, 1, n_}] :=
      Sum[-(-1)^k (x-1)^k/k, {k, 1, n}] +
      O[x, 1]^(n+1)
```

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CIRCLE NO. 107

Use Spice to analyze component variations in circuit designs

George Ellis, Kaydon Corp

If you already use Spice to simulate circuits, you can easily use Monte Carlo methods to investigate the effects of component variation on circuit performance. Modifying your circuit models to do this analysis is only a matter of adding a few lines.

In the hectic process of design, simulation, prototyping, and testing, it's easy to neglect variations in circuit components. If you do consider variations, you may add some margin to nominal component values and yet be guided by only a rule of thumb or an educated guess. Then, component tolerances can stack up the wrong way and yield unpleasant results.

It's possible, though, to accurately account for component tolerances without expending extraordinary effort. Spice, the most popular circuit simulator today, provides a variety of tools for analyzing component variations. The most powerful of these tools is Monte Carlo analysis.

Circuit performance varies because parameter values vary. The variations either can be deterministic or statistical. Deterministic variations are possible to predict. For example, the resistance of copper is deterministic: It increases about 0.39% for every °C of temperature increase. The effect is the same, for all practical purposes, from one piece of copper to the next.

It's not possible, however, to predict precisely the effects of statistical variations on any given component. Examples of statistical variations include manufacturing tolerance (the variation of values from one unit to the next) and aging (the variation of values over time). Fortunately, you can analyze statistical variations with Spice.

If you're uncomfortable working with statistical variation, it may be because the analysis tools seem mysterious. However, if you already use Spice to simulate your circuits, you may be surprised to learn how easily Spice can simulate variations. In fact, you will probably need to make only a few modifications to your circuit models to investigate the most important sources of variation.

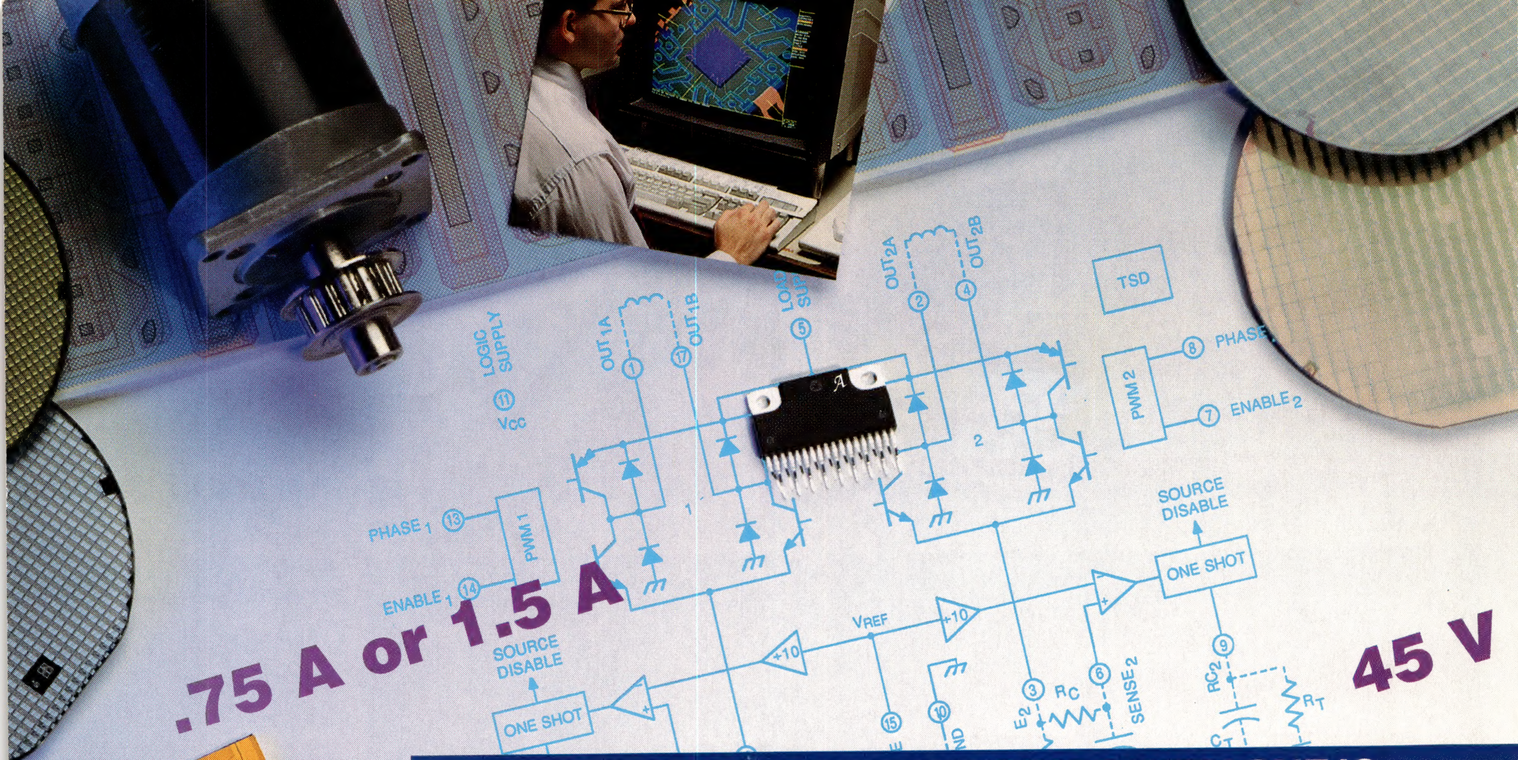
The examples presented here use PSpice (**Refs 1 and 2**), a version of Spice from Microsim Corp. The implementation of variation analysis differs among Spice versions, but the principles are the same. You should be able to apply this information to any version of Spice that offers statistical-variation analysis.

PSpice lets you add a tolerance value to any parameter by using the DEV directive in the .MODEL command. For example, you can specify a 1%, 20-kΩ resistor with these two lines:

```
R1 1 2 ONE_PERCENT_R 20K
.MODEL ONE_PERCENT_R RES(R=1 DEV=1%)
```

When you simulate the circuit, the "ONE_PERCENT_R" in the specification for R1 will point PSpice to a model named ONE_PERCENT_R, which shows that R, the resistance multiplier, has a 1% device tolerance. (Incidentally, the character string "ONE_PERCENT_R" has no meaning itself; any name would have worked.)

The DEV directive can apply to any parameter in


.75 A or 1.5 A
45 V
LOGIC SUPPLY
OUT 1A
OUT 1B
OUT 2A
OUT 2B
TSD
PHASE 2
ENABLE 2
PWM 2
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